B.S. Abdur Rahman®
Crescent
Institute of Science & Technology
Deemed to be University u/s 3 of the UGC Act, 1956

Regulations 2025
Curriculum and Syllabi
(Updated as per 25th Academic Council – March 2026)

M.Tech.
(VLSI and Embedded Systems)

B.S. Abdur Rahman® Crescent Institute of Science & Technology
Deemed to be University u/s 3 of the UGC Act, 1956

REGULATIONS 2025

CURRICULUM AND SYLLABI

(Updated as per 25th Academic Council – March 2026)

M.TECH. VLSI AND EMBEDDED SYSTEMS

VISION AND MISSION OF THE INSTITUTION

VISION

B.S. Abdur Rahman Crescent Institute of Science and Technology aspires to be a leader in Education, Training and Research in multidisciplinary areas of importance and to play a vital role in the Socio- Economic progress of the Country in a sustainable manner.

MISSION

- To blossom into an internationally renowned Institute.
- To empower the youth through quality and value-based education.
- To promote professional leadership and entrepreneurship.
- To achieve excellence in all its endeavors to face global challenges.
- To provide excellent teaching and research ambience.
- To network with global Institutions of Excellence, Business, Industry and Research Organizations.
- To contribute to the knowledge base through Scientific enquiry, Applied Research and Innovation.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Department of Electronics and Communication Engineering envisions to be a leader in providing state of the art education through excellence in teaching, training, and research in contemporary areas of Electronics and Communication Engineering and aspires to meet the global and socio economic challenges of the country.

MISSION

The Department of Electronics and Communication Engineering, endeavours to produce globally competent Engineers prepared to face challenges of the society.

- To enable the students to formulate, design and solve problems in applied science and engineering.
- To provide excellent teaching and research environment using state of the art facilities.
- To provide adequate practical training to meet the requirement of the Electronics & communication industry.
- To train the students to take up leadership roles in their career or to pursue higher education and research

PROGRAMME EDUCATIONAL OBJECTIVES AND OUTCOMES

M.TECH. VLSI AND EMBEDDED SYSTEMS

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: To design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design

PEO2: To apply the knowledge of software and hardware tools related to the design and implementation of integrated Circuits, Systems for real time embedded applications

PEO3: To carry out research in various domains and to work in the VLSI and Embedded Systems related industries

PEO4: To work effectively as a team and manage projects in multidisciplinary environments.

PROGRAMME OUTCOMES

PO1: An ability to independently carry out research/investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program.

PO4: Ability to design and conduct experiments, perform analysis, applying the knowledge of computing, mathematics, science and electronic engineering for designing VLSI and Embedded Systems.

PO5: Interpret the problems of VLSI and Embedded Systems and investigate solutions and work towards improved solutions.

PO6: Continuously update knowledge with modern tools and technical developments and ensure professional development.

PROGRAMME SPECIFIC OUTCOMES

PSO1: Be able to analyze, design and implement Analog, Digital and Mixed Signal Circuits and real time embedded systems

PSO 2: Have in-depth knowledge and capability to use industry standard tools in the design and implementation of VLSI and real time Embedded Systems.

PSO 3: Be able to undertake research projects and work as a team in the related domains of VLSI and Embedded systems.

B.S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE AND TECHNOLOGY, CHENNAI – 600 048.

REGULATIONS 2025

M.Tech. / MCA / M.Sc. / M.Com. / M.A. DEGREE PROGRAMMES

(Under Choice Based Credit System)

(Amendments as approved by the 25th Academic Council – March 2026)

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires:

i) **"Programme"** means post graduate degree programme (M.Tech. / MCA / M.Sc. / M.Com. / M.A.)

ii) **"Branch"** means specialization or discipline of programme like M.Tech. in Structural Engineering, Food Biotechnology etc., M.Sc. in Physics, Chemistry, Actuarial Science, Biotechnology etc.

iii) **"Course"** means a theory / practical / laboratory integrated theory / mini project / seminar / internship / project and any other subject that is normally studied in a semester like Advanced Concrete Technology, Electro Optic Systems, Financial Reporting and Accounting, Analytical Chemistry, etc.

iv) **"Institution"** means B.S. Abdur Rahman Crescent Institute of Science and Technology.

v) **"Academic Council"** means the Academic Council, which is the apex body on all academic matters of this Institute.

vi) **"Dean (Academic Affairs)"** means the Dean (Academic Affairs) of the Institution who is responsible for the implementation of relevant rules and regulations for all the academic activities.

vii) **"Dean (Student Affairs**)" means the Dean (Students Affairs) of the Institution who is responsible for activities related to student welfare, conduct of co-curricular, extra-curricular events and discipline in the campus.

viii) **"Controller of Examinations"** means the Controller of Examinations of the Institution who is responsible for the conduct of examinations and declaration of results.

ix) **"Dean of the School"** means the Dean of the School of the department concerned.

x) **"Head of the Department"** means the Head of the Department concerned.

2.0 ADMISSION REQUIREMENTS

2.1 Students for admission to the first semester of the Master's Degree Programme shall be required to have passed the appropriate degree examination as specified in the clause 3.2 [Eligible entry qualifications for admission to programmes] of this Institution or any other University or authority accepted by this Institution.

2.2 The other conditions for admission such as class obtained, number of attempts in the qualifying examination and physical fitness will be as prescribed by the Institution from time to time.

3.0 BRANCHES OF STUDY

3.1 The various programmes and their mode of study are as follows:

Degree	Mode of Study
M.Tech.	Full Time
MCA	
M.Sc.	
M.Com.	
M.A.	

3.2 Programmes offered

S. No.	Name of the Department	Programmes offered
1.	Aeronautical Engineering	M.Tech. (Avionics)
2.	Civil Engineering	M.Tech. (Structural Engineering)
		M. Tech. (Construction Engineering and Project Management)
3.	Mechanical Engineering	M.Tech. (CAD/CAM)
4.	Electrical and Electronics Engineering	M.Tech. (Power Systems Engineering)
5.	Electronics and Communication	M.Tech. (VLSI and Embedded Systems)

S. No.	Name of the Department	Programmes offered
	Engineering	
6.	Computer Science and Engineering	M.Tech. (Computer Science and Engineering)
		M.Tech. (Artificial Intelligence and Data Science)
7.	Information Technology	M.Tech. (Information Technology)
8.	Computer Applications	MCA
9.	Mathematics	M.Sc. (Actuarial Science)
10.	Physics	M.Sc.(Physics)
11.	Chemistry	M.Sc.(Chemistry)
12.	Life Sciences	M.Sc. Biochemistry & Molecular Biology
		M.Sc. Biotechnology
		M.Sc. Microbiology
		M.Sc. Stem Cell Technology
		M.Sc. Clinical Embryology
		M.Tech. Biotechnology
		M.Tech. Food Biotechnology
13.	Commerce	M.Com
14.	Arabic and Islamic Studies	M.A. Islamic Studies

3.3 Eligible entry qualifications for admission to programmes

Sl. No.	Programme	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
1.	M.Tech. (Avionics)	B.E. / B.Tech. in Aeronautical Engineering / Aerospace Engineering / Mechanical Engineering / Mechatronics / EEE / ECE / EIE / or Equivalent degree in relevant field.
2.	M.Tech. (Structural Engineering)	B.E. / B.Tech. in Civil Engineering / Structural Engineering or Equivalent degree in relevant field.

Sl. No.	Programme	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
	M. Tech. (Construction Engineering and Project Management)	B.Tech. in Mechanical / Civil / Electrical and Electronics / Geo Informatics / B Plan / B. Des, and B.Arch.
3.	M.Tech. (CAD/CAM)	B.E. / B.Tech. in Mechanical / Automobile / Manufacturing / Production / Industrial / Mechatronics / Metallurgy / Aerospace / Aeronautical / Material Science / Polymer / Plastics / Marine Engineering or Equivalent degree in relevant field.
4.	M.Tech. (Power Systems Engineering)	B.E. / B.Tech. in EEE / ECE / EIE / ICE / Electronics / Instrumentation Engineering or Equivalent degree in relevant field.
5.	M.Tech. (VLSI and Embedded Systems)	B.E. / B.Tech. in ECE / EIE / ICE / EEE / IT or Equivalent degree in relevant field.
6.	M.Tech. (Computer Science and Engineering)	B.E. / B.Tech. in CSE / IT / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.
	M.Tech. (Artificial Intelligence and Data Science)	B.E. / B.Tech. in CSE / IT / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.
7.	M.Tech. (Information Technology)	B.E. / B.Tech. in IT / CSE / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.
8.	MCA	BCA / B.Sc. Computer Science / B.E. / B.Tech. / B.Sc. Mathematics, B.Sc. Physics / Chemistry / B.Com. / BBA / B.A. with Mathematics at graduation level or at 10 + 2level or equivalent degree in relevant field.
9.	M.Sc. (Actuarial Science)	Any under graduate degree with Mathematics / Statistics as one of the subjects of study at 10 + 2 level.
10.	M.Sc.(Physics)	B.Sc. in Physics / Applied Science / Electronics /Electronics Science / Electronics & Instrumentation or Equivalent degree in relevant field.

Sl. No.	Programme	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
11.	M.Sc.(Chemistry)	B.Sc. in Chemistry / Applied Science or Equivalent degree in relevant field.
12.	M.Sc. Biochemistry & Molecular Biology	B.Sc. in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
	M.Sc. Biotechnology	B.Sc. in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
	M.Sc. Microbiology	B.Sc.in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
	M.Sc. Stem Cell Technology	B.Sc.in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
	M.Sc. Clinical Embryology	B.Sc.in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
	M.Tech. Biotechnology	B.Tech. / B.E. in Biotechnology or Equivalent degree in relevant field.
	M.Tech. Food Biotechnology	B.E. / B.Tech. in Biotechnology / Food Biotechnology / Chemical Engineering / Biochemical Engineering / Industrial Biotechnology or Equivalent degree in relevant field.
13. .	M.Com	B.Com. / BBA
14. .	M.A. Islamic Studies	B.A. in Islamic Studies / Arabic (or) Afzal-ul-Ulama (or) Any under graduate degree with Part 1 Arabic (or)

Sl. No.	Programme	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
		Any under graduate degree with Aalim Sanad / Diploma / Certificate in Arabic or Islamic Studies.

4.0. STRUCTURE OF THE PROGRAMME

4.1. The PG. programmes consist of the following components as prescribed in the respective curriculum:

i. Core courses
ii. Elective courses
iii. Laboratory integrated theory courses
iv. Project work
v. Laboratory courses
vi. Open elective courses
vii. Seminar
viii. Mini Project
ix. Industry Internship
x. MOOC courses (NPTEL- Swayam, Coursera etc.)
xi. Value added courses

4.1.1. The curriculum and syllabi of all programmes shall be approved by the Academic Council of this Institution.

4.1.2. For the award of the degree, the student has to earn a minimum total credits specified in the curriculum of the respective specialization of the programme.

4.1.3. The curriculum of programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below:

Programme	Range of credits
M.Tech.	80 - 86
MCA	80 - 86
M.Sc.	80 - 85
M.Com.	80 - 88
M.A.	80 - 84

4.1.4. Credits will be assigned to the courses for all programmes as given below:

- ❖ One credit for one lecture period per week or 15 periods of lecture per semester.
- ❖ One credit for one tutorial period per week or 15 periods per semester.
- ❖ One credit each for seminar/practical session/project of two or three periods per week or 30 periods per semester.
- ❖ One credit for 160 hours of industry internship per semester for all programmes (except M.Com.)
- ❖ Four credits for 160 hours of industry internship per semester for M.Com.

4.1.5. The number of credits the student shall enroll in a non-project semester and project semester is as specified below to facilitate implementation of Choice Based Credit System.

Programme	Non-project semester	Project semester
M.Tech.	9 to 32	18 to 26
MCA	9 to 32	18 to 26
M.Sc.	9 to 32	10 to 26
M.Com.	9 to 32	16 to 28
M.A.	9 to 32	NA

4.1.6 The student may choose a course prescribed in the curriculum from any department offering that course without affecting regular class schedule. The attendance will be maintained course wise only.

4.1.7 The students shall choose the electives from the curriculum with the approval of the Head of the Department / Dean of School.

4.1.8 Apart from the various elective courses listed in the curriculum for each specialization of programme, the student can choose a maximum of two electives from any other similar programmes across departments, alter to open electives, during the entire period of study, with approval of Head of the department offering the course and parent department.

4.1.9. Online Courses through SWAYAM and Other MOOC Platforms: Credit Transfer and Curriculum Integration

Students are permitted to undergo Department-approved online courses offered through the SWAYAM platform up to 40% of the total credits prescribed in a semester, excluding the project semester,

during their period of study, with the recommendation of the Head of the Department/Dean of the School and prior approval of the Dean (Academic Affairs). The credits earned through such online courses, after approval/ratification by the respective Board of Studies, shall be transferred following the prescribed approval procedures. These online courses may be considered in lieu of Core Courses and Elective Courses, subject to equivalence and approval by the competent authorities.

Students shall also be permitted to undergo online courses offered through recognized Massive Open Online Course (MOOC) platforms other than SWAYAM, such as Coursera, Udemy, and other equivalent platforms approved by the University, to enable students across all disciplines to gain global academic exposure, acquire industry-relevant skills, and enhance employability.

The online courses offered through such platforms may be mapped either partially or fully with the curriculum of the respective programme, subject to the approval of the Department/Programme Committee concerned. The Departments may integrate such online courses as components of courses prescribed in the curriculum. In such cases, the successful completion of the prescribed online course and the certification obtained thereof may be considered as a component of the Continuous/Internal Assessment of the respective course, as recommended by the Class Committee and approved by the competent authority.

4.1.10 Project work

Project work shall be carried out by the student under the supervision of a faculty member in the department with similar specialization.

A student may however, in certain cases, be permitted to work for the project in an Industry / Research organization, with the approval of the Head of the Department/ Dean of School. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist / Competent authority from the organization and

the student shall be instructed to meet the faculty periodically and to attend the review meetings for evaluating the progress.

The timeline for submission of final project report / dissertation is within 30 calendar days from the last instructional day of the semester in which project is done.

If a student does not comply with the submission of project report / dissertation on or before the specified timeline he / she is deemed to have not completed the project work and shall re-register in the subsequent semester.

5.0 DURATION OF THE PROGRAMME

5.1. The minimum and maximum period for completion of the programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M.Tech.	4	8
MCA	4	8
M.Sc.	4	8
M.Com.	4	8
M.A.	4	8

5.2 Each academic semester shall normally comprise of 90 working days. Semester end examinations shall follow within 10 days of the last Instructional day.

5.3 Medium of instruction, examinations and project report shall be in English.

6.0 REGISTRATION AND ENROLLMENT

6.1 The students of first semester shall register and enroll at the time of admission by paying the prescribed fees. For the subsequent semesters registration for the courses shall be done by the student one week before the last working day of the previous semester.

6.2 Change of a Elective Course

A student can change an enrolled elective course within 10 working days from the commencement of the course, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

6.3 Withdrawal from a Course

A student can withdraw from an enrolled course at any time before the first continuous assessment test for genuine reasons, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

6.4 A student can enroll for a maximum of 36 credits during a semester including Redo / Predo courses.

7.0 BREAK OF STUDY FROM PROGRAMME

7.1 A student may be allowed / enforced to take a break of study for two semesters from the programme with the approval of Dean (Academic Affairs) for the following reasons:

7.1.1 Medical or other valid grounds

7.1.2 Award of 'I' grade in all the courses in a semester due to lack of attendance

7.1.3 Debarred due to any act of indiscipline

7.2 The total duration for completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1).

7.3 A student who has availed a break of study in the current semester (odd/even) can rejoin only in the subsequent corresponding (odd/even) semester in the next academic year on approval from the Dean (Academic affairs).

7.4 During the break of study, the student shall not be allowed to attend any regular classes or participate in any activities of the Institution. However, he / she shall be permitted to enroll for the 'I' grade courses and appear for the arrear examinations.

8.0 CLASS ADVISOR AND FACULTY ADVISOR

8.1 CLASS ADVISOR

A faculty member shall be nominated by the HOD/ Dean of School as Class Advisor for the class throughout their period of study.

The class advisor shall be responsible for maintaining the academic, curricular and co-curricular records of students of the class throughout their period of study.

8.2 FACULTY ADVISOR

To help the students in planning their courses of study and for general counseling, the Head of the Department / Dean of School of the students shall attach a maximum of 20 students to a faculty member of the department who shall function as faculty advisor for the students throughout their period of study. Such faculty advisor shall guide the students in taking up the elective courses for registration and enrolment in every semester and also offer advice to the students on academic and related personal matters.

9.0 COURSE COMMITTEE

9.1 Each common theory / laboratory course offered to more than one group of students shall have a “Course Committee” comprising all the teachers handling the common course with one of them nominated as course coordinator. The nomination of the course coordinator shall be made by the Head of the Department / Dean (Academic Affairs) depending upon whether all the teachers handling the common course belong to a single department or from several departments. The Course Committee shall meet as often as possible to prepare a common question paper, scheme of evaluation and ensure uniform evaluation of the assessment tests and semester end examination.

10.0 CLASS COMMITTEE

10.1 A class committee comprising faculty members handling the courses, student representatives and a senior faculty member not handling any courses for that class as chairman will be constituted in every semester:

10.2 The composition of the class committee will be as follows:

i) One senior faculty member preferably not handling courses for the concerned semester, appointed as chairman by the Head of the Department
ii) Faculty members of all courses of the semester
iii) All the students of the class
iv) Faculty advisor and class advisor
v) Head of the Department – Ex officio member

10.3 The class committee shall meet at least three times during the semester. The first meeting shall be held within two weeks from the

date of commencement of classes, in which the nature of continuous assessment for various courses and the weightages for each component of assessment shall be decided for the first and second assessment. The second meeting shall be held within a week after the date of first assessment report, to review the students' performance and for follow up action.

10.4 During these two meetings the student members, shall meaningfully interact and express opinions and suggestions to improve the effectiveness of the teaching-learning process, curriculum and syllabi of courses.

10.5 The third meeting of the class committee, excluding the student members, shall meet within 5 days from the last day of the semester end examination to analyze the performance of the students in all the components of assessments and decide their grades in each course. The grades for a common course shall be decided by the concerned course committee and shall be presented to the class committee(s) by the concerned course coordinator.

11.0 CREDIT REQUIREMENTS TO REGISTER FOR PROJECT WORK

11.1 A student is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	Minimum no. of credits to be earned to enroll for project semester
M.Tech.	18
MCA	22
M.Sc.	18
M.Com	NA
M.A.	NA

11.2 If the student has not earned minimum number of credits specified, he/she has to earn the required credits, at least to the extent of minimum credits specified in clause 9.1 and then register for the project semester.

12.0 ASSESSMENT PROCEDURE AND PERCENTAGE WEIGHTAGE OF MARKS

12.1 Every theory course shall have a total of three assessments during a semester as given below:

Assessments	Weightage of Marks
Continuous Assessment 1	25%
Continuous Assessment 2	25%
Semester End Examination	50%

12.2 Theory Course

Appearing for semester end theory examination for each course is mandatory and a student shall secure a minimum of 40% marks in each course in semester end examination for the successful completion of the course.

12.3 Laboratory Course

Every practical course shall have 75% weightage for continuous assessments and 25% for semester end examination. However, a student shall have secured a minimum of 50% marks in the semester end practical examination for the award of pass grade.

12.4 Laboratory Integrated Theory (LIT) Courses

For laboratory integrated theory courses, the theory and practical components shall be assessed separately for 100 marks each and consolidated by assigning a weightage of 75% for theory component and 25% for practical component (for a 4 credit LIT Course). Grading shall be done for this consolidated mark. Assessment of theory components shall have a total of three assessments with two continuous assessments carrying 25% weightage each and semester end examination carrying 50% weightage. The student shall secure a separate minimum of 40% in the semester end theory examination. The evaluation of practical components shall be through continuous assessment.

Component	Maximum Marks	Weightage for Final Grade	Mode of Assessment

Theory Component	100	75%	CAT1 (25%) + CAT2 (25%) + SEE (50%)
Practical Component	100	25%	60% Continuous assessment + 40% End Semester exam
Final Grade Basis	Consolidated	100%	75% Theory + 25% Practical
Pass Requirement	-	-	Minimum 40% in Semester-End Theory Exam (SEE)

Note:

1. Proportionate weightage shall be assigned to LIT courses based on their credit value, whether 2 or 3 credits.
2. In Lab-Integrated Professional Elective courses, the laboratory component shall be assessed by the course faculty.

12.5 The components of continuous assessment the theory/ practical/ laboratory integrated theory courses shall be finalized in the first class committee meeting.

12.6 Industry Internship/ Start-up Activity

In the case of industry internship/ start-up activity, the student shall submit a report, which shall be evaluated along with an oral examination by a committee of faculty members constituted by the Head of the Department. The student shall also submit an internship completion certificate issued by the industry / CIIC / research / academic organization. The weightage of marks for industry internship/ start-up activity report and viva voce examination shall be 60% and 40% respectively.

12.7 Project Work

Mini Project / Start-up Project shall be carried out either individually or as a group activity involving a maximum of four students. Each group shall identify a suitable problem, project, or start-up idea within their domain, either disciplinary or interdisciplinary, in consultation with the

faculty mentor. The project shall lead to the development of a prototype, model, application or other innovation-driven outcome.

The progress of the Mini Project / Start-up Project shall be evaluated through three periodic reviews comprising two interim reviews and one final review. A project report shall be submitted at the end of the semester. The reviews shall be conducted by a committee of faculty members constituted by the Head of the Department/Dean of the School. An oral examination (Viva Voce) shall be conducted as the semester-end examination by an internal examiner approved by the Controller of Examinations based on the project report.

The weightage for assessment shall be:

- Periodic Reviews – 50%
  - 25% by the Project Guide
  - 25% by the Review Committee
- Project Report – 20%
- Viva Voce Examination – 30%

The Project / Start-up Project shall be carried out either individually or as a group activity involving a maximum of four students. The project shall demonstrate the student's ability to integrate and apply the knowledge and skills acquired throughout the programme to address a real-world problem, research challenge, innovation, or entrepreneurial opportunity.

A committee of faculty members constituted by the Head of the Department/Dean of the School shall conduct three periodic reviews during the semester to monitor and assess the progress of the project. At the end of the semester, students shall submit a project report, based on which a semester-end Viva Voce examination shall be conducted by an external examiner approved by the Controller of Examinations.

The weightage for assessment shall be:

- Periodic Reviews – 50%
  - 25% by the Project Guide

25% by the Review Committee

- Project Report – 20%
- Viva Voce Examination – 30%

12.8 Interdisciplinary Project Work

To promote innovation, multidisciplinary learning, entrepreneurship, and start-up-oriented project development, students shall be encouraged to undertake interdisciplinary project work involving participation from at least two different Departments, Schools, or Programmes.

An interdisciplinary project team may consist of a minimum of two and a maximum of four students from two or more disciplines, subject to the norms prescribed by the University from time to time. Each interdisciplinary project shall be guided by a Supervisor from one participating discipline and a Co-Supervisor from another participating discipline.

The project proposal shall clearly define the interdisciplinary nature of the work and specify the roles and responsibilities of the participating students. The proposal shall be approved by the concerned Department/Programme Committee(s) before the commencement of the project.

The evaluation of students shall be carried out by the respective departments/programmes in accordance with the regulations applicable to the concerned programme. Each student shall be assessed primarily on the contribution made towards the objectives related to his/her discipline, while also contributing to the overall objectives and outcomes of the interdisciplinary project.

The implementation, evaluation, and other procedural aspects of interdisciplinary project work shall be in accordance with the Standard Operating Procedure (SOP) prescribed by the University.

12.9 The assessment of seminar course including its component and its weightage shall be decided by a committee of faculty members constituted by the Head of the Department. This committee shall ensure the conduct of assessment of components and award marks

accordingly.

12.10 For the first attempt of the arrear theory examination, the internal assessment marks scored for a course during first appearance shall be used for grading along with the marks scored in the arrear examination. From the subsequent appearance onwards, full weightage shall be assigned to the marks scored in the semester end examination and the internal assessment marks secured during the course of study shall become invalid.

12.11 In case of laboratory integrated theory courses, after one regular and one arrear appearance, the internal mark of theory component is invalid and full weightage shall be assigned to the marks scored in the semester end examination for theory component. **There shall be no arrear or improvement examination for lab components**.

13.0 SUBSTITUTE EXAMINATIONS

13.1 A student who is absent, for genuine reasons, may be permitted to write a substitute examination for any one of the two continuous assessment tests of a course by paying the prescribed substitute examination fee. However, permission to take up a substitute examination will be given under exceptional circumstances, such as accidents, admission to a hospital due to illness, etc. by a committee constituted by the Head of the Department / Dean of School for that purpose. However, there is no substitute examination for semester end examination.

13.2 A student shall apply for substitute exam in the prescribed form to the Head of the Department / Dean of School within a week from the date of assessment test. However, the substitute examination will be conducted only after the last working day of the semester and before the semester end examination.

14.0 ATTENDANCE REQUIREMENT AND SEMESTER / COURSE REPETITION

14.1 A student shall earn 100% attendance in the scheduled contact hours (such as lectures, tutorials, labs, etc.) for that course. However, a relaxation of up to 25% in attendance may be granted to account for valid reasons such as medical emergencies, participation in co-curricular or extracurricular activities with prior approval, or other genuine circumstances.

If a student's attendance falls below 75% in a particular course, even after considering the permissible relaxation, they will not be allowed to appear for the semester-end examination in that course. Instead, the student will be awarded an “I” grade (Incomplete) for the course

14.2 The faculty member of each course shall cumulate the attendance details for the semester and furnish the names of the students who have not earned the required attendance in the concerned course to the class advisor. The class advisor shall consolidate and furnish the list of students who have earned less than 75% attendance, in various courses, to the Dean (Academic Affairs) through the Head of the Department / Dean of the School. Thereupon, the Dean (Academic Affairs) shall officially notify the names of such students prevented from writing the semester end examination in each course.

14.3 If a student’s attendance in any course falls between 65% and 75% due to medical reasons (e.g., hospitalization, illness) or participation in institution-approved events, they may be granted exemption from the minimum attendance requirement and allowed to appear for the semester-end exam. The student must submit valid documents to the class advisor upon rejoining, with approval from the HoD/Dean. Final approval for **condonation** will be granted by the Vice Chancellor based on the Dean (Academic Affairs)’s recommendation.

14.4 A student who has obtained an “I” grade in all the courses in a semester is not permitted to move to the next higher semester. Such students shall **repeat** all the courses of the semester in the subsequent academic year. However, he / she is permitted to redo the courses awarded with 'I' grade / arrear in previous semesters. They shall also be permitted to write arrear examinations by paying the prescribed fee.

14.5 The student awarded “I” grade, shall enroll and repeat the course when it is offered next. In case of “I” grade in an elective course either the same elective course may be repeated or a new elective course may be taken with the approval of the Head of the Department / Dean of the School.

14.6 A student who is awarded “U” grade in a course shall have the option to either write the semester end arrear examination at the end of the subsequent semesters, or to **redo** the course when the course is offered by the department. Marks scored in the continuous assessment in the redo course shall be considered for grading along with the marks scored

in the semester end (redo) examination. If any student obtains "U" grade in the redo course, the marks scored in the continuous assessment test (redo) for that course shall be considered as internal mark for further appearance of arrear examination.

14.7 If a student with "U" grade, who **prefers to redo** any particular course, fails to earn the minimum 75% attendance while doing that course, then he / she is not permitted to write the semester end examination and his / her earlier "U" grade and continuous assessment marks shall continue.

a. Students engaged in approved and verifiable start-up activities may be granted an additional relaxation of up to 15% in attendance requirements, subject to the recommendation of the Crescent Innovation and Incubation Council (CIIC) and approval of the Head of the Department/Dean of the School concerned.

15.0 REDO / PRE-DO COURSES

15.1 A student can register for a maximum of three redo courses per semester without affecting the regular semester classes, whenever such courses are offered by the concerned department, based on the availability of faculty members and subject to a specified minimum number of students registering for each of such courses.

15.2 The number of contact hours and the assessment procedure for any redo course shall be the same as regular courses, except there is **no provision for any substitute examination and withdrawal from a redo course**.

15.3 A student shall be permitted to pre-do a course offered by the concerned department, provided it does not affect the regular semester class schedule. Such permission shall be granted based on the availability of faculty members, the maximum permissible credit limit of the semester, and the student's fulfillment of the necessary prerequisites for the course. The proposal shall be recommended by the Dean of the School and the Head of the Department, and shall require final approval from the Dean (Academic Affairs).

16.0 PASSING AND DECLARATION OF RESULTS AND GRADE SHEET

16.1 All assessments of a course shall be made on absolute marks basis. The class committee without the student members shall meet to analyse the performance of students in all assessments of a course and award letter grades following the relative grading system. The letter grades and the corresponding grade points are as follows:

Letter Grade	Grade Points
S	10
A	9
B	8
C	7
D	6
E	5
U	0
W	-
I	-
PA	-
FA	-

"W"- denotes withdrawal from the course

“I” - denotes “Incomplete” ie. inadequate attendance in the course and prevention from appearance of semester end examination

“U” - denotes unsuccessful performance in the course.

“PA” - denotes the ‘Pass’ of the zero credit courses.

“FA” - denotes the ‘Fail’ of the zero credit courses.

16.2 A student who earns a minimum of five grade points (‘E’ grade) in a course is declared to have successfully completed the course. Such a course cannot be **repeated by the student for improvement of grade**.

16.3 Upon awarding grades, the results shall be endorsed by the chairman of the class committee and Head of the Department / Dean of the

School. The Controller of Examinations shall further approve and declare the results.

16.4 **Within one week** from the date of declaration of result, a student can apply for revaluation of his / her semester end theory examination answer scripts of one or more courses, on payment of prescribed fee, through proper application to the Controller of Examinations. Subsequently, the Head of the Department / Dean of the School offered the course shall constitute a revaluation committee consisting of chairman of the class committee as convener, the faculty member of the course and a senior faculty member having expertise in that course as members. The committee shall meet within a week to revalue the answer scripts and submit its report to the Controller of Examinations for consideration and decision.

16.5 After results are declared, grade sheets shall be issued to each student, which contains the following details: a) list of courses enrolled during the semester including redo courses / arrear courses, if any; b) grades scored; c) Grade Point Average (GPA) for the semester and d) Cumulative Grade Point Average (CGPA) of all courses enrolled from the first semester onwards.

GPA is the ratio of the sum of the products of the number of credits of courses registered and the grade points corresponding to the grades scored in those courses, taken for all the courses, to the sum of the number of credits of all the courses in the semester.

If C_i, is the number of credits assigned for the i^{th} course and GP_i is the Grade Point in the i^{th} course,

$$GPA = \frac{\sum_{i=1}^{n}(C_i)(GPi)}{\sum_{i=1}^{n} C_i}$$

Where n = number of courses

The Cumulative Grade Point Average (CGPA) is calculated in a similar manner, considering all the courses enrolled from first semester.

“I”, "W", “PA” and **“FA”** grades are excluded for calculating GPA.

"U", “I”, "W", “PA” and **“FA”** grades are excluded for calculating CGPA.

The formula for the conversion of CGPA to equivalent percentage of marks shall be as follows:

Percentage equivalent of marks = CGPA X 10

16.6 After successful completion of the programme, the degree shall be awarded to the students with the following classifications based on CGPA.

Classification	CGPA
First Class with Distinction	8.50 and above and passing all the courses in first appearance and completing the programme within the prescribed period of 8 semesters for all students (except lateral entry students) and 6 semesters for lateral entry students
First Class	6.50 and above and completing the programme within a maximum of 10 semesters for all students (except lateral entry students) and 8 semesters for lateral entry students
Second Class	Others

16.6.1 Eligibility for First Class with Distinction

- A student should not have obtained 'U' or 'I' grade in any course during his/her study
- A student should have completed the UG programme within the minimum prescribed period of study (except clause 7.1.1)

16.6.2 Eligibility for First Class

- A student should have passed the examination in all the courses not more than two semesters beyond the minimum prescribed period of study (except clause 7.1.1)

16.6.3 The students who do not satisfy clause 16.6.1 and clause 16.6.2 shall be classified as second class.

16.6.4 The CGPA shall be rounded to two decimal places for the purpose

of classification. The CGPA shall be considered up to three decimal places for the purpose of comparison of performance of students and ranking.

17.0 SUPPLEMENTARY EXAMINATION

Final year students and passed out students can apply for supplementary examination for a maximum of **three** courses thus providing an opportunity to complete their degree programme. The students can apply for supplementary examination within three weeks of the declaration of results in the even semester.

18.0 DISCIPLINE

18.1 Every student is expected to observe discipline and decorum both inside and outside the campus and not to indulge in any activity which tends to affect the reputation of the Institution.

18.2 Any act of indiscipline of a student, reported to the Dean (Student Affairs), through the Head of the Department / Dean of the School concerned shall be referred to a Discipline and Welfare Committee constituted by the Registrar for taking appropriate action.

19.0 MULTI ENTRY AND MULTI EXIT (MEME) FRAMEWORK *

In accordance with the provisions of the National Education Policy (NEP) 2020, the programme shall support a Multi Entry – Multi Exit (ME-ME) framework to provide flexibility in the academic pathway of students.

***At present (AY 2025-26), it is applicable only for all M.Tech. Programmes.**

19.1. Exit Option:

19.1.1 Credit Requirement for Award of M.Tech. Degree

To qualify for the award of a M.Tech. degree from the Institute, a

student must successfully complete the total credit requirements as prescribed in the approved curriculum of the respective programme. The specific credit requirements are determined by the programme curriculum.

19.1.2 Provision for Multiple Exit

In alignment with NEP 2020 guidelines, the Institute provides students enrolled in postgraduate programmes with the option of multiple exits, subject to the following conditions:

a. Exit at the End of First Year

Students may choose to exit the programme at the end of the first year, provided they have fulfilled the prescribed academic requirements.

b. Application for Exit

A student intending to exit must submit a formal written application in the prescribed format at least **eight weeks prior to the scheduled end of the academic year.**

c. Departmental Recommendation

1. Upon receipt of the application, the concerned Department shall evaluate the academic record of the student and recommend the award of a **Post Graduate Diploma**, based on the credits earned.

2. In the case of arrear courses, the post graduate diploma will be conferred only after successful clearance of all pending arrears.

d. Notification of Completion

Once a student has fulfilled the requirements for the award of post graduate diploma, the Department shall notify the same to controller of examinations for further processing and issuance.

19.1.3 Award of Qualifications under Multiple Exit Scheme

Post graduate diploma: Awarded after successful completion of the first year, subject to earning the prescribed cumulative credits as per the respective programme curriculum (e.g., 44 credits from the first year) along with 3 credits of Skill Based Courses.

19.1.4 Conditions Governing Exit

1. The multiple exit facility is intended strictly for **genuine and exceptional circumstances,** such as prolonged illness, or securing an employment opportunity necessitating a temporary withdrawal from the programme.
2. Students opting for a temporary exit after the first year must obtain **prior approval from the Registrar through Dean (Academics),** based on the recommendation of the respective Head of the Department.

19.1.5 Expectation of Programme Continuity

While the option for multiple exits exists, it is generally expected that students admitted to a post graduate programme shall pursue their studies continuously until completion of the final degree requirements.

19.2. Entry Option:

Students seeking re-entry into the programme (multi-entry) must submit an application through the proper channel at the beginning of the odd semester. Admission shall be subject to fulfilment of institutional guidelines, credit mapping, and availability of seats.

19.3. Credits Requirement for the Certifications

Name of the Certificate Programme	Required Credits
Post graduate Diploma (Level 6.5 as per NEP 2020)	40* - 45

* The minimum number of credits that a student must earn (as per the respective curriculum) in order to get the above certification program

20.0 ELIGIBILITY FOR THE AWARD OF THE MASTER'S DEGREE

20.1 A student shall be declared to be eligible for the award of the Master's Degree, if he/she has:

i. Successfully acquired the required credits as specified in the curriculum corresponding to his/her programme within the maximum period of 8 semesters from the date of admission, including break of study.
ii. No disciplinary action is pending against him/her.

iii. Enrolled and completed at least one value added course.

iv. Enrollment in at least one MOOC / SWAYAM course (non-credit) before the final semester.

20.2 The award of the degree must have been approved by the Institute.

21.0 POWER TO MODIFY

Notwithstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

****

B. S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE AND TECHNOLOGY

M.TECH. VLSI AND EMBEDDED SYSTEMS

CURRICULUM & SYLLABI, REGULATIONS 2025

(Choice Based Credit System)

SEMESTER I

Sl. No.	Course Category	Course Code	Course Title	L	T	P	C
1	BS	MAF 6183	Probability, Optimization and Matrix Theory	3	1	0	4
2	PCC	ECF 6121	Digital VLSI Design	3	0	0	3
3	PCC	ECF 6122	Advanced Embedded System and Programming	3	0	0	3
4	PCC	ECF 6123	VLSI Verification Methodologies	3	0	0	3
5	PCC	ECF 6124	Embedded Processor Architectures and Programming	3	0	2	4
6	PCC	ECF 6125	Digital VLSI Design and Verification Laboratory	0	0	2	1
7	PEC		Professional Elective	3	0	0	3
			Credits				**21**

SEMESTER II

Sl. No.	Course Category	Course Code	Course Title	L	T	P	C
1	ES	GEF 6201	Research Methodology and IPR for Engineers	2	0	0	2
2	PCC	ECF 6221	Real Time Operating Systems	3	0	0	3
3	PCC	ECF 6222	Analog Integrated Circuit Design	3	0	2	4
4	PCC	ECF 6223	Embedded LINUX	2	0	2	3
5	PCC	ECF 6224	Embedded Systems Laboratory	0	0	2	1
6	PEC		Professional Elective	3	0	0	3
7	PEC		Professional Elective	3	0	0	3
8	HS	ENF 6281	Professional Communication	0	0	2	1
9		ECF 6225	Mini Project	0	0	6	3

Credits 23

SEMESTER III

Sl. No.	Course Category	Course Code	Course Title	L	T	P	C
1	OEC	OEC	Open Elective	3	0	0	3
2	PCC	ECF 7121	Mixed Signal Integrated Circuits	3	0	0	3
3	PEC		Professional Elective Courses	3	0	0	3
4	PEC		Professional Elective Courses	3	0	0	3
5	Internship	ECF 7122	Industry Internship *	0	0	4	2
6	Project	ECF 7123	Project Work – Phase I #	0	0	14	7
7	MOOC		MOOC (Related to project) **				
			Credits				**14**

SEMESTER IV

Sl. No.	Course Category	Course Code	Course Title	L	T	P	C
1	Project	ECF 7123	Project Work – Phase II	0	0	35	18
			Credits				**18**
			Total Credits				**25(18+7)**
			Overall Total Credits				**83**

* Industrial training will be undertaken during the summer vacation of first-year for 30 days. The credit will be awarded in the 3rd Semester.

Credits for Project Work Phase I to be accounted along with Project Work Phase II in IV Semester

** The students shall pursue a MOOC course related to the project in the third semester, and the progress in this regard shall be monitored during Project Phase – I reviews.

Enrollment and completed at least one value-added course is mandatory.

PROFESSIONAL ELECTIVE COURSES

VLSI DESIGN

Sl. No.	Course Group	Course Code	Course Title	L	T	P	C
1.	PEC	ECFY 001	Low Power IC Design	3	0	0	3
2.	PEC	ECFY 002	ASIC Design	3	0	0	3
3.	PEC	ECFY 003	Testing of VLSI Circuits	3	0	3	3
4.	PEC	ECFY 004	Scripting Languages for VLSI Design Automation	3	0	0	3
5.	PEC	ECFY 005	RF Integrated Circuit Design	3	0	0	3
6.	PEC	ECFY 006	VLSI Digital Signal Processing	3	0	0	3
7.	PEC	ECFY 007	Quantum Computing	3	0	0	3

EMBEDDED SYSTEM

Sl. No.	Course Group	Course Code	Course Title	L	T	P	C
1.	PEC	ECFY 008	Embedded System for Robotics	3	0	0	3
2.	PEC	ECFY 009	Embedded Automotive Systems	3	0	0	3
3.	PEC	ECFY 010	Artificial Intelligence	3	0	0	3
4.	PEC	ECFY 011	Industrial IoT	3	0	0	3
5.	PEC	ECFY 012	Machine Learning and Deep Learning for Embedded System	3	0	0	3
6.	PEC	ECFY 013	Real Time Systems	3	0	0	3
7.	PEC	ECFY 014	Multicore Architecture	3	0	0	3
8.	PEC	ECFY 015	Modern Antenna Theory and Applications	3	0	0	3
9.	PEC	ECFY 016	Nano Electronics and Technology	3	0	0	3
10.	PEC	ECFY 017	Advanced Biomedical Signal Processing	3	0	0	3

LIST OF OPEN ELECTIVE COURSES FOR

M.TECH. PROGRAMMES – REGULATIONS 2025 –
OFFERED IN III SEMESTER

Sl. No.	Course Code	Course Title	L	T	P	C	Offering Department
1.	OEFY 701	Alternative Energy Resources	3	0	0	3	Chemistry
2.	OEFY 702	Analytical Techniques	3	0	0	3	Chemistry
3.	OEFY 703	Artificial Intelligence and IoT	3	0	0	3	CSE
4.	OEFY 704	Artificial Intelligence in Healthcare and Biotechnology	3	0	0	3	SLS
5.	OEFY 705	Biomass for Energy Applications	3	0	0	3	Chemistry
6.	OEFY 706	Biomedical Engineering Fundamentals	3	0	0	3	SLS
7.	OEFY 707	Biosensors and Diagnostic Technologies	3	0	0	3	SLS
8.	OEFY 708	Corrosion and its Control	3	0	0	3	Chemistry
9.	OEFY 709	Data Science and Machine	3	0	0	3	IT
10.	OEFY 710	Electric Vehicle and Battery Storage Technology	3	0	0	3	EEE
11.	OEFY 711	Environmental Chemistry	3	0	0	3	Chemistry
12.	OEFY 712	Environmental Sustainability and Green Building Practices	3	0	0	3	Civil Engineering
13.	OEFY 713	Fuel Cells for Sustainable Energy Production	3	0	0	3	Chemistry
14.	OEFY 714	Green and Sustainable Chemistry	3	0	0	3	Chemistry
15.	OEFY 715	Industrial Pollution Control	3	0	0	3	Chemistry
16.	OEFY 716	Introduction to Quantum	3	0	0	3	Physics
17.	OEFY 717	Materials for Energy Applications	3	0	0	3	Physics
18.	OEFY 718	Nanotechnology and Catalysis	3	0	0	3	Chemistry
19.	OEFY 719	Project Management	3	0	0	3	Mechanical
20.	OEFY 720	Real Time Embedded Systems	3	0	0	3	ECE
21.	OEFY 721	Renewable Energy Systems	3	0	0	3	EEE

22.	OEFY 722	Surface Coating Technology	3	0	0	3	Chemistry
23.	OEFY 723	Thin film Science and Technology	3	0	0	3	Physics
24.	OEFY 724	Advanced Project Management	3	0	0	3	Mechanical

SEMESTER I

MAF 6183	**PROBABILITY, OPTIMIZATION AND**	**L**	**T**	**P**	**C**
SDG: 04	**MATRIX THEORY**	**3**	**1**	**0**	**4**

COURSE OBJECTIVES:

COB1: To carry out probability calculations and identify probability distributions.

COB2: To gain the knowledge of the multidimensional random variables.

COB3: To formulate and solve linear programming, transportation, and assignment problem.

COB4: To apply matrix factorizations (LU, Cholesky, QR, SVD) and pseudo-inverse for linear systems.

COB5: To solve variational problems including higher-order and constrained cases using Euler's method.

MODULE I RANDOM VARIABLE AND DISTRIBUTIONS L:9 T:3 P:0

Random variable – Expectations – Moments – Variances – Binomial, Poisson, Geometric, Negative Binomial, Uniform, Exponential, Gamma, Normal distributions.

MODULE II MULTIDIMENSIONAL RANDOM VARIABLES L:9 T:3 P:0

Joint distributions – Marginal and conditional distributions – Covariance – Correlation and Regression – Partial, multiple correlations and regressions.

MODULE III OPTIMIZATION TECHNIQUES L:9 T:3 P:0

Linear Programming – Formulation – Simplex method and duality – Transportation problems – Assignment problems.

MODULE IV MATRIX DECOMPOSITION TECHNIQUES L:9 T:3 P:0

Matrix norms – Singular value decomposition – LU decomposition – Cholesky decomposition – QR decomposition – Pseudo inverse.

MODULE V CALCULUS OF VARIATIONS L:9 T:3 P:0

Variation and its properties – Euler's equation – Functional dependent on first and higher order derivatives – Functional dependent on functions of several independent variables – Variational problems with moving boundaries – Isoperimetric problems.

L – 45; T – 15; TOTAL HOURS – 60

TEXT BOOKS:

1. Sheldon M. Ross, "Introduction to Probability and Statistics for Engineers and Scientists", 6th Edition,, Academic Press, 2020
2. Richard A. Johnson, "Probability and Statistics for Engineers", 9th Edition, Pearson, 2017.
3. Hamdy A. Taha, "Operations Research: An Introduction", 11th Ediion, Pearson, 2022.
4. David W. Lewis, "Matrix Theory", Allied Publishers (Chennai), 2011 reprint of 1995 work.
5. A. S. Gupta, "Calculus of Variations with Applications", PHI, 2011.

REFERENCES:

1. T. Veerarajan, "Probability, Statistics and Random Processes", 3rd Edition, McGraw Hill, 2008.
2. Gupta and V.K. Kapoor, "Fundamentals of Mathematical Statistics", 12th Edition., Sultan Chand, 2014.
3. Horn and Johnson, "Matrix Analysis", 2nd Edition, Cambridge, 2012.
4. Hillier and Lieberman, "Introduction to Operations Research", 10th Edition, McGraw Hill, 2014.

COURSE OUTCOMES: At the end of the course students will be able to

CO1: select and use appropriate discrete and continuous probability models for engineering data.

CO2: analyze multidimensional distributions, calculate covariance, correlation, and perform regressions

CO3: translate real-world problems into LP models and solve them via simplex, dual, transportation, and assignment methods.

CO4: decompose matrices (LU, Cholesky, QR, SVD), compute pseudo-inverses, and apply to least-squares solutions.

CO5: formulate and solve calculus of variations problems—including isoperimetric and boundary-moving cases—using Euler's equations.

Board of Studies (BOS):
17th BOS of Department of Mathematics and Actuarial Science held on 23.06.2025.

Academic Council:
24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	2	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-

*** Legend: L – Low (1), M – Medium (2), H – High (3).**

SDG 4 – Quality Education: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Learning of probability, distributions and calculus of variations will lead to knowledge of applications in Engineering.

ECF 6121	DIGITAL VLSI DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Explain the physical principles of MOS devices and fabrication processes

COB2: Analyse CMOS logic design styles and delay/power characteristics

COB3: Design and simulate combinational and sequential digital systems

COB4: Employ subsystem-level design and performance enhancement techniques

COB5: Understand timing issues, interconnect effects, and memory design principles

MODULE I THE MOS TRANSISTOR L:9 T:0 P:0

Semiconductor concepts: Silicon, doping – P-N junction – CMOS transistor – Threshold voltage – I-V characteristics – Channel length modulation – Velocity saturation – Subthreshold leakage – DIBL – GIDL – Short channel effects. CMOS inverter: Static and dynamic characteristics. Fabrication technologies: Crystal growth – Wafer preparation – Oxidation – Ion implantation – Lithography – Etching – Metallization – Packaging – CMOS process flow.

MODULE II CMOS LOGIC DESIGN AND FINITE STATE MACHINES L:9 T:0 P:0

Logic design styles: Static CMOS – Pass transistor logic – Transmission gates – Complex gates.

Sequential logic: SR latch, D-latch, edge-triggered flip-flops – Timing and non-ideal effects.

Dynamic logic: Domino and NORA logic. Finite State Machines (FSMs): Mealy and Moore models – FSM implementation using CMOS – Timing constraints – Use in control logic. Clocking issues: Two-phase clocking – Clock skew – Setup/hold time.

MODULE III SUBSYSTEM DESIGN AND PIPELINING L:9 T:0 P:0

Design styles: Ratioed logic (Pseudo-NMOS, DCVSL) – Differential logic. Arithmetic building blocks: Adders (Ripple, Carry Look-Ahead), Multipliers – Booth

and Wallace tree – Barrel shifters. Power in logic design: Dynamic, static, and short-circuit power. Pipelining: Concept, latch-based design – Throughput and latency optimization.

Register-transfer level (RTL) implementation.

MODULE IV INTERCONNECTS, TIMING AND SYNCHRONIZATION **L:9 T:0 P:0**

Interconnect modelling: R, C, and L – Wire delay models – Elmore delay. Timing metrics: Path delay, slack, setup/hold margins – Static timing analysis. Synchronous vs. asynchronous systems – Self-timed logic – Synchronizers, metastability. Clock generation: PLL, DLL – Clock distribution and skew minimization.

MODULE V MEMORY DESIGN AND ADVANCED STRUCTURES **L:9 T:0 P:0**

Memory cell design: SRAM – DRAM – ROM – Bit cell optimization. Peripheral circuits: Row/column decoders, sense amplifiers, write drivers. Array architecture: Wordline/bitline optimization – Memory hierarchy. Reliability: Soft errors, redundancy techniques – Yield improvement. Low power memory techniques – Emerging memory (RRAM, MRAM) overview.

L – 45; Total Hours:45

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic,“Digital Integrated Circuits: A Design Perspective”, Second Edition, PHI, 2016.
2. Neil H.E. Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Fifth Edition, Pearson Education, 2022.
3. David Money Harris, Sarah L. Harris, “Digital Design and Computer Architecture”, ARM Edition, Second Edition, Morgan Kaufmann, 2015.

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Second Edition, Oxford University Press, 2023.
2. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits – Analysis and Design”, Fourth Edition, McGraw-Hill, 2015.

3. Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, Fourth Edition, Wiley-IEEE Press, 2019.
4. N. Weste, D. Harris, “CMOS VLSI Design” (Solutions Manual), Pearson, 2022.

COURSE OUTCOMES:

CO1: Describe CMOS device characteristics and fabrication steps

CO2: Design and simulate logic circuits using static and dynamic CMOS styles

CO3: Implement FSMs and optimize sequential circuits

CO4: Apply pipelining and subsystem-level design in VLSI circuits

CO5: Evaluate timing, interconnect, and memory performance in digital systems

Board of Studies (BoS):
27th BOS of Department of ECE held on 26.06.2025

Academic Council:
24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3						3		
CO2	3		3		2		3	3	
CO3	3		3		2		3	3	
CO4	3		3		2		3	3	
CO5	3			2	2		3	2	

*** Legend: L – Low (1), M – Medium (2), H – High (3).**

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement:

Learning Digital VLSI Design enables students with advanced knowledge in VLSI design, promoting academic and industrial competency.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement:

Knowledge of Digital VLSI concepts supports innovation in semiconductor design and digital infrastructure development.

ECF 6122	ADVANCED EMBEDDED SYSTEMS	L	T	P	C
SDG: 4,9	AND PROGRAMMING	3	0	0	3

COURSE OBJECTIVES:

COB1: To outline the phases of embedded system design and demonstrate methodologies for hardware/software partitioning and low-power system architecture.

COB2: To explain the operation of legacy and modern communication protocols and illustrate their implementation in embedded systems.

COB3: To develop embedded software using appropriate toolchains and apply debugging, simulation, and integration techniques,

COB4: To implement programming constructs in Embedded C and Python and apply data structures for efficient embedded application development.

COB5: To evaluate component choices and design embedded solutions aligned with current trends in IoT, AI, and edge computing environments.

MODULE I EMBEDDED SYSTEM DESIGN L:9 T:0 P:0

Embedded Design Life Cycle-Product Specification- Hardware / Software Partitioning-Detailed Hardware and Software Design- System Integration-Product Testing-Component Selection in the Context of IoT and AI Workloads-Embedded Platform Boot Sequence-Low-Power Design and Power Optimization Techniques -DVFS- sleep modes.

MODULE II EMBEDDED COMMUNICATION INTERFACES AND INTERRUPT HANDLING MECHANISMS L:9 T:0 P:0

I/O Device Ports & Buses-Serial Bus Communication: RS232, RS485, USB, I²C, SPI-CAN Bus and Industrial Interfaces-Modern Communication Protocols: MQTT, BLE, Zigbee- Interrupts, Exceptions, Context Switching-Interrupt Latency and Deadlines-Introduction to Device Drivers

.

MODULE III EMBEDDED SOFTWARE DEVELOPMENT AND TOOLCHAINS **L:9 T:0 P:0**

Embedded Software Development Environment-IDEs, Assemblers, Compilers, Linkers, Simulators-Debuggers and In-Circuit Emulators-Assembly Linking and Loading-Basic Compilation Techniques-Program Optimization Methods.

MODULE IV EMBEDDED C AND DATA STRUCTURES **L:9 T:0 P:0**

Introduction to Embedded C vs Traditional C-Data Types, Control Structures, Loops-Strings, Arrays, Pointers, and Functions- Bitwise and Logical Operators-Efficient Memory Usage in Embedded Systems- Data Structures in Embedded Context - Stacks, Queues, Linked Lists-Trees, Heaps, Graphs- Searching and Sorting Algorithms.

MODULE V EMBEDDED PYTHON AND EDGE COMPUTING APPLICATIONS **L:9 T:0 P:0**

Python Programming Fundamentals- Data Types, Operators, Control Statements-Functions and Modular Programming- Introduction to SoC Platforms -Sensor Interfacing with SoC- Embedded Python: Micro Python and Circuit Python- Simple Edge AI Applications using Python- Cloud Connectivity for IoT (e.g., Firebase, Things Board).

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Marilyn Wolf, "Computers as components", Elsevier 4th edition 2016
2. Designing Embedded Systems and the Internet of Things (IoT) with the ARM Cortex-M Microcontrollers" Author: Perry Xiao Publisher: Wiley
3. Practical Python Programming for IoT "Author: Gary Smart Publisher: Apress
4. Python for Microcontrollers: Getting Started with Micro Python"– Donald Norris

REFERENCES:

1. Embedded Systems: Introduction to ARM® Cortex™-M Microcontrollers" 6th Edition,2019, Jonathan W. Valvano.
2. Peter Barry, Patrick Crowley, "Modern Embedded Computing" Morgan Kaufmann Publishers, 2012.

COURSE OUTCOMES:

CO1: Describe the stages of the embedded system design process and evaluate key design consideration

CO2: Demonstrate the ability to configure and implement communication protocols like RS232, I2C, and CAN for embedded networking.

CO3: Develop and optimize embedded software using IDEs, simulators, and debugging tools.

CO4: Write structured programs in Embedded C and apply appropriate data structures to solve embedded system problems.

CO5: Create Python-based embedded applications with sensor interfacing and basic SoC programming.

Board of Studies (BoS):
27th BOS of Department of ECE held on 26.06.2025

Academic Council:
24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	1	3	2	3	1	3	2	2
CO2	1	–	3	3	3	–	3	3	–
CO3	2	1	3	3	2	3	2	3	2
CO4	1	–	3	3	3	–	3	3	–
CO5	2	1	3	3	2	3	3	2	3

*** Legend: L – Low (1), M – Medium (2), H – High (3).**

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement:
Learning Digital VLSI Design enables students with advanced knowledge in VLSI design, promoting academic and industrial competency.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement:

Knowledge of Digital VLSI concepts supports innovation in semiconductor design and digital infrastructure development

ECF 6123	VLSI VERIFICATION METHODOLOGIES	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: Introduce Verification Techniques

COB2: Understand the concept of classes and create objects

COB3: Design techniques using system Verilog

COB4: Establish verification environment using system Verilog

COB5: Introduce advanced concepts of OOPS

MODULE I INTRODUCTION TO VERIFICATION TECHNIQUES **L:9 T:0 P:0**

The Verification Methodology, Basic Testbench Functionality, Directed Testing, Methodology Basics Constrained-Random Stimulus, Randomize, Functional Coverage, Testbench Components, Layered Testbench, Building a Layered Testbench, Built-In Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods, Choosing a Storage Type, Creating User-Defined Structures, Packages, Type Conversion, Streaming Operators, Enumerated Types, Constants, Strings, Expression Width.

MODULE II PROCEDURAL STATEMENTS AND ROUTINES **L:9 T: 0 P:0**

Procedural Statements, Tasks, Functions, Void Functions, Task and Function, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values, Separating the Testbench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, Program Block Considerations, Connecting It All Together, Top-Level Scope, Program–Module Interactions, The Four-Port ATM Router, The Ref Port Direction.

MODULE III BASIC OOP **L:9 T: 0 P:0**

OOP Terminology, Creating New, Object De-allocation, Using Objects, Class Methods, Defining Methods Outside of the Class, Static Variables vs. Global Variables, Scoping Rules, Using One Class Inside Another, Understanding Dynamic

Objects, Arrays of Handles, Copying Objects, Public vs. Local, Straying Off Course, Building a Testbench.

MODULE IV RANDOMIZATION L:9 T: P:0

Randomization in System Verilog, Constraint Details, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post_randomize Functions

MODULE V ADVANCED OOP AND TESTBENCH GUIDELINES L:9 T :0 P:0

Working with Threads, Disabling Threads, Interprocess Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC, Introduction to Inheritance, Blueprint Pattern, Downcasting and Virtual Methods, Composition, Inheritance, and Alternatives, Copying an Object, Abstract Classes and Pure Virtual Methods, Callbacks, Parameterized Classes, Static and Singleton Classes, Creating a Test Registry.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Tumbush, Greg. Systemverilog for Verification-a Guide to Learning the Testbench Language. Springer-verlag New York Incorporated, 2012.
2. Mehta, Ashok B. Introduction to SystemVerilog. Springer Nature, 2021.SrivatsaVasudevan, Practical UVM: Step by Step with IEEE 1800.2, R. R. Bowker, 2020.

REFERENCES:

1. Cooper, Vanessa R. Getting Started with UVM: A Beginner's Guide. Vol. 22. Austin: Verilab Publishing, 2013.
2. Cerny, Eduard, SurrendraDudani, John Havlicek, and Dmitry Korchemny. SVA: the power of assertions in systemVerilog. Springer International Publishing, 2015.
3. Zwolinski, Mark. Digital system design with SystemVerilog. Pearson Education, 2009.

COURSE OUTCOMES:

CO1: Understand VLSI verification Techniques

CO2: Learn to create objects

CO3: Develop testbench with system verilog

CO4: Create a verification environment

CO5: Develop system Verilog models for verification with advanced OOPS concepts

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	-	-	3	2	3	1
CO2	1	-	2	-	-	2	2	2	1
CO3	2	2	3	-	-	3	3	3	2
CO4	3	2	3	-	-	3	3	3	3
CO5	3	2	3	-	-	3	3	3	3

*** Legend: L – Low (1), M – Medium (2), H – High (3).**

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement: Develop a standard verification environment

ECF 6124	**EMBEDDED PROCESSOR**	**L**	**T**	**P**	**C**
SDG: 4,9	**ARCHITECTURES AND PROGRAMMING**	**3**	**0**	**2**	**4**

COURSE OBJECTIVES:

COB1: To know Microcontroller based system design, applications.

COB2: To teach I/O interface in system Design.

COB3: To learn about Design and programming of MSP 430 microcontroller.

COB4: To study the ARM architecture and program.

COB5: To involve the students to Practice on Workbench /Software Tools/ Hardware Processor Boards with the supporting Peripherals.

MODULE I PIC MICROCONTROLLER ARCHITECTURE L:9 T:0 P:3

Architecture – memory organization – addressing modes –Overview instruction set - I/O ports-bank switching, I/O Programming-Timer programming- ADC, DAC and Sensor interfacing, Practice in MPLAB compiler.

MODULE II MSP430 ARCHITECTURE AND PROGRAMMING L:9 T:0 P:3

Architecture, CPU features – Memory Structures – Addressing Modes – Instruction sets – Interrupts programming – Input and Output Programming – On-Chip Peripherals – Flash Memory – Low Power design – Practice in IAR workbench.

MODULE III ARM ARCHITECTURE AND PROGRAMMING L:9 T:0 P:3

ARM Architecture-LPC2148- The ARM Programmer's model - Instruction set – Thumb instruction set – I/O Programming –UART programming- ADC-DAC-I2C Programming-Bit manipulation and Bit Shifting –USB communication.

MODULE IV ARM CORTEX M3 L:9 T:0 P:3

Overview of the Cortex-M3- Registers- Special Registers- Instruction Sets- Memory Systems- programming on- chip peripherals.

MODULE V SYSTEM DESIGN – CASE STUDY L:9 T:0 P:3

Interfacing LCD Display – Keypad Interfacing - Motor Control – Controlling DC/ AC appliances – Stand-alone Data Acquisition System.

L – 45; T – 0; P – 30; Total Hours:75

TEXT BOOKS:

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey “PIC Microcontroller and Embedded Systems using Assembly and C for PIC18”, Pearson Education 2008
2. John Iovine, “PIC Microcontroller Project Book”, McGraw Hill 2000
3. Rajkamal, “Microcontrollers Architecture, Programming, Interfacing & System Design”, Pearson, 2012
4. Joseph Yiu, “The Definitive guide to ARM Cortex-M3”, Elsevier, 3rd Edition,2014

REFERENCES:

1. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier 2003.
2. Steve Furber, ARM System on Chip Architecture, Addison –Wesley Professional, 2014.

COURSE OUTCOMES:

CO1: Create ALP and C programs to develop applications using 8051 & PIC Microcontroller.

CO2: Debugging the embedded programs under KEIL µvision and MPLAB IDE

CO3: Describe the architecture of MSP series of microcontroller

CO4: Create ALP and C programs to develop applications using the MSP430 Microcontroller.

CO5: Interface the internal and External IOs of PIC, MSP and ARM processor.

CO6: Use KEIL µvision IDE,IAR Embedded workbench and MPLAB IDE.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1		PSO2	PSO3
CO1	3	-	3	2	1	-	2		1	2
CO2	3	2	3	2	2	-	2		-	2
CO3	3	-	3	2	1	-	3		-	2
CO4	3	2	3	2	2	-	3		-	2
CO5	3	-	3	2	1	-	3		-	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Embedded processor knowledge will provide useful information for high-quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement : able to advance industrialization through the use of embedded processor concepts

ECF 6125	**DIGITAL VLSI DESIGN AND**	**L**	**T**	**P**	**C**
SDG: 9	**VERIFICATION LABORATORY**	**0**	**0**	**2**	**1**

COURSE OBJECTIVES:

COB1: Design and implement combinational and sequential logic circuits using appropriate digital design principles and tools.

COB2: Apply Finite State Machine (FSM) design techniques to model and analyse complex digital systems.

COB3: Design memory units and real-time digital systems such as a time-of-day clock using systematic approaches.

COB4: Use System Verilog constructs to develop and simulate digital circuits, focusing on data types, procedural blocks, and routines.

COB5: Implement verification techniques using System Verilog, including test bench integration, constrained randomization, and functional coverage.

Cycle I **Introduction to Verification techniques** **L:6 T:0 P:6**

Design of Combinational circuits

Design of sequential Circuits.

Finite State Machine Design Technique

Design of Memory Circuits

Design a Time of day clock

Cycle 2 **System Verilog for verification** **L:6 T:0 P:8**

Declaring, initializing and using different data types.

Develop Procedural Statements and Routines

Connecting Testbench and Design

Randomization

Functional Coverage

P – 30; Total Hours:30

TEXT BOOKS:

1. Tumbush, Greg. Systemverilog for Verification-a Guide to Learning the Testbench Language. Springer-verlag New York Incorporated, 2012.
2. Mehta, Ashok B. Introduction to SystemVerilog. Springer Nature, 2021.
3. SrivatsaVasudevan, Vasudevan, Srivatsa, Practical UVM: Step by Step with IEEE 1800.2, R. R. Bowker, 2020

REFERENCES:

1. Cooper, Vanessa R. Getting Started with UVM: A Beginner's Guide. Vol. 22. Austin: Verilab Publishing, 2013.
2. Cerny, Eduard, SurrendraDudani, John Havlicek, and Dmitry Korchemny. SVA: the power of assertions in systemVerilog. Springer International Publishing, 2015.
3. Zwolinski, Mark. Digital system design with SystemVerilog. Pearson Education, 2009.

COURSE OUTCOMES:

CO1: Design and implement combinational and sequential circuits using standard digital logic components and simulation tools.

CO2: Apply Finite State Machine (FSM) design methodologies to develop and analyze control-based digital systems.arn to create objects

CO3: Design and simulate memory-based circuits and real-time digital applications such as a time-of-day clock.

CO4: Develop and verify digital designs using SystemVerilog, demonstrating proficiency in data types, procedural constructs, and modular design.

CO5: Apply verification techniques such as testbench creation, constrained randomization, and functional coverage to validate digital systems.

Board of Studies (BoS): 27th BO

S of Department of ECE held on 26.06.2025

Academic Council:

24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	1		3	3			3	2	
CO2	1		3		3		3	2	
CO3	2		3	3			3	2	
CO4	2		3	3	3	3	3	2	
CO5	3		3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement: Develop a standard verification environment

SEMESTER II

GEF 6201	**RESEARCH METHODOLOGY AND IPR FOR**	**L**	**T**	**P**	**C**
SDG: 4, 8, 9	**ENGINEERS**	**2**	**0**	**0**	**2**

COURSE OBJECTIVES:

COB1: To apply a perspective on research

COB2: To select the appropriate statistical techniques for hypothesis construction and methods of data analysis and interpretation

COB3: To analyze the research design by using optimization techniques.

COB4: To describe the research findings as research reports, publications, copyrights Patenting and Intellectual Property Rights.

MODULE I RESEARCH PROBLEM FORMULATION AND RESEARCH DESIGN **8**

Research - objectives – types - Research process, solving engineering problems -Identification of research topic - Formulation of the research problem, literature survey and review. Research design - meaning and need - basic concepts - Different research designs, Experimental design - principle, Design of experimental setup, Mathematical modeling - Simulation, validation, and experimentation.

MODULE II DATA COLLECTION, ANALYSIS AND INTERPRETATION OF DATA **8**

Sources of Data, Use of the Internet in Research, Types of Data - Research Data Processing and analysis - Interpretation of results- Correlation with scientific facts - repeatability and reproducibility of results - Accuracy and precision –limitations, Application of Computer in Research- Importance of statistics in research - Sample design. Hypothesis testing, ANOVA, Design of experiments - Factorial designs - Orthogonal arrays.

MODULE III OPTIMIZATION TECHNIQUES **6**

Use of optimization techniques - Traditional methods – Evolutionary Optimization Techniques. Multivariate analysis Techniques, Classifications, Characteristics, Applications - correlation and regression, Curve fitting.

MODULE IV INTELLECTUAL PROPERTY RIGHTS **8**

The Research Report - Purpose of the written report - Synopsis writing - preparing papers for International Journals, Software for paper formatting like LaTeX/MS Office, Reference Management Software, Software for detection of Plagiarism – Thesis writing, - Organization of contents - style of writing- graphs, charts, and Presentation tool - Referencing, Oral presentation, and defense - Ethics in research - Patenting, Intellectual Property Rights - Patents, Industrial Designs, Copyrights, Trade Marks, Geographical Indications-Validity of IPR, Method of Patenting, procedures, Patent Search

L – 30; Total Hours: 30

TEXT BOOKS:

1. Ganesan R., “Research Methodology for Engineers”, MJP Publishers, Chennai, 2011.
2. George E. Dieter., “Engineering Design”, McGraw Hill – International edition, 2020.
3. Kothari C.R., “Research Methodology” – Methods and Techniques, New Age International (P) Ltd, New Delhi, 2020.
4. Kalyanmoy Deb., “Genetic Algorithms for optimization”, Kangal report, No.2001002.
5. Rajkumar S. Adukia, “Handbook on Intellectual Property Rights in India”, TMH Publishers, 2020.

REFERENCES:

1. Holeman, J.P., ”Experimental methods for Engineers, Tata McGraw Hill Publishing Co., Ltd., New Delhi, 2017.
2.Govt. of India, ”Intellectual Property Laws; Acts, Rules & Regulations”, Universal Law Publishing Co. Pvt. Ltd., New Delhi 2020.
3. R Radha Krishnan & S Balasubramanian, “Intellectual Property Rights”. 1st Edition, Excel Books, 2012.
4.Derek Bosworth and Elizabeth Webster. “The Management of Intellectual Property”, Edward Elgar Publishing Ltd., 2013

COURSE OUTCOMES:

At the end of the course, the student should be able to:

COB1: Formulate the research problem

COB2: Design and Analyse the research methodology

COB3: Analyse and interpret the data to construct and optimize the research hypothesis

COB4: Report the research findings as publications, copyright, trademarks and IPR

Board of Studies (BoS) : 20th BoS of Civil held on 08.07.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4
CO1	3	**I**	**2**	**1**
CO2	2	3	**3**	**2**
CO3	3	2	2	3
CO4	**1**	3	2	**2**

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Analysis and design of core field design promotes engineering skills and quality education.

Statement: This course enables the student to analyze the existing technology for further solution and its qualitative measures in terms of societal requirements.

SDG 8: Development of new technologies with core field design provides sustainable economic growth and productive employment.

Statement: To apply the hybrid techniques and concepts for different applications provides sustainable economic growth and productive employment.

SDG 9: Creative and curiosity of core field design fosters innovation and sustainable industrialization.

Statement: This course plays major roles through innovative ideas in industry towards modern infrastructures and sustainability.

ECF 6221	REAL TIME OPERATING SYSTEMS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Introduce the concepts of Operating systems and Real-time Operating Systems

COB2: Impart knowledge on Resource management, time-constrained communication, scheduling and imprecise computations, real-time kernels and case studies.

COB3: Learn the kernel architecture of µC/OS-II RTOS

COB4: Compare various RTOS

COB5: Apply RTOS for control Systems

MODULE I REVIEW OF OPERATING SYSTEMS L:9 T: 0 P:0

Introduction- operating system services and structures-system calls- process management-process synchronization-classical synchronization problem-CPU scheduling.

MODULE II REAL TIME OPERATING SYSTEM AND SCHEDULING L:9 T:0 P: 0

Real-time System-Basic model-characteristics-safely,reliability-types-Timing constraints-Real time task scheduling-classification-clock driven-hybrid schedulers-Event driven scheduling –EDF –RMA-issues.

MODULE III IPC IN RTOS L:9 T:0 P: 0

Resource sharing –priority inversion-priority inheritance protocol-Highest Locker Protocol-Priority Ceiling Protocol-different types of priority inversions under PCP-Feature-issues in IPC protocol-Handling Task Dependencies

MODULE IV µC/OS-II RTOS L:9 T:0 P: 0

Introduction – Features-Kernel Structures- Task Management – Time Management- Event Control Block- Semaphores- Memory Management- Porting RTOS

MODULE V COMMERCIAL RTOS AND APPLICATION **L:9 T:0 P: 0**

Comparison and study of various RTOS –VRTX-QNX – VX works – RT Linux Case studies-RTOS for fault Tolerant Applications – RTOS for Control Systems.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Rajib Mall, Real-Time Systems: Theory and Practice, Pearson, 2009
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
3. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.

REFERENCES:

1. Silberschatz,Galvin,Gagne” Operating System Concepts,6th ed,John Wiley,2003
2. D.M.Dhamdhere,” Operating Systems,A Concept-Based Approch,TMH,2008
3. Charles Crowley, “Operating Systems-A Design Oriented approach” Tata McGraw Hill,1996 .

COURSE OUTCOMES:

CO1: Illustrate OS structure and explain process scheduling types.

CO2: Compare the features of traditional OS and RTOS.

CO3: Describe inter task communication and synchronization mechanisms

CO4: Analyze and design real time scheduling algorithms

CO5: Select appropriate RTOS for the required application.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2		2	2			2		
CO2	2	3	3		2		3	3	2
CO3	2	2	3	3	2		3	3	3
CO4	3	2	3	3	3		2	3	3
CO5	2	3	3		3	2	3	3	

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Real-time operating system knowledge will provide useful information for high-quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement: able to advance industrialization through the use of real-time operating system concepts.

ECF 6222	ANALOG INTEGRATED CIRCUIT DESIGN	L	T	P	C
SDG: 9		3	0	2	4

COURSE OBJECTIVES:

COB1: Understand the Design and Analysis of MOS Amplifiers

COB2: Analyse and Design Differential Amplifiers

COB3: Implement Current Mirrors and Biasing Techniques

COB4: Evaluate Frequency Response of Analog Circuits

COB5: Design and Analyze Operational Amplifiers and Phase-Locked Loops

MODULE I **MOS Amplifier design** **L:6 T:0 P:6**

Single Stage Amplifiers: Common-Source Stage, Source Follower, Common-Gate Stage, Cascode-Stage. Differential Amplifiers: Single-Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, differential Pair with MOS Loads, Gilbert Cell

Lab : Design and Analysis of MOS Single-Stage and Differential Amplifiers

MODULE II **Current Mirrors and Biasing Techniques** **L:6 T:0 P:6**

Basic Current Mirrors, Cascode Current Mirrors, Active current Mirrors, Biasing Techniques.

Lab: Design and Simulation of Current Mirrors and Biasing Techniques Using MOSFETs

MODULE III **Frequency Response of Amplifiers** **L: 6 T:0 P:6**

Millller Effect, Common source stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair, Gain-Bandwidth trade-Offs.

Lab: Frequency Response Analysis of MOSFET Amplifier Configurations and Gain-Bandwidth Trade-Offs

MODULE IV Operational Amplifiers L: 6 T: 0 P:6

One-Stage OPAMPS, Two-Stage OPAMPS, Gain Boosting, Output Swing Calculations, Common-Mode Feedback, Input Range Limitations, Slew rate, High-Slew-Rate, Power Supply Rejection, Noise in OPAMPS

Lab: Design and Performance Analysis of CMOS Operational Amplifiers

MODULE V Phase-Locked Loops L: 6 T: 0 P:6

Simple PLL, Charge-Pump PLLs, Nonideal Effects in PLLs, Delay-Locked Loops, Applications.

Lab: Design and Analysis of Phase-Locked Loops and Delay-Locked Loops

L – 45; T – 0; P – 30; Total Hours:75

TEXT BOOKS:

1. BehzadRazavi, “Design of analog CMOS integrated circuits”, 2nd Edition, McGraw Hill, 2017
2. Allen, Holberg, “CMOS analog circuit design”, 3rd Edition, Oxford University Press, 2012
3. David A. Bell, “Electronic Devices and Circuits”, 5th ed., Oxford University Press, 2015

REFERENCES:

1. Sergio Franco, “Design with Operational amplifiers and Analog Integrated circuits”, 4th ed., Tata McGraw-Hill, 2016
2. Ramakant A. Gayakwad, “Op-amp and Linear ICs”, 4th ed., Printice Hall/Pearson, Education,2015
3. Gray, Meyer, Lewis, Hurst, “Analysis and design of Analog Integrated Circuits”, 5th Edition, Willey International, 2009.

COURSE OUTCOMES:

CO1: Analyse and design various MOS amplifier configurations

CO2: Design and evaluate differential amplifier circuits, including differential pairs with active loads and the Gilbert Cell

CO3: Implement and analyse different types of current mirrors and biasing techniques to ensure proper bias stability in analog circuit design.

CO4: Evaluate the frequency response of amplifier stages considering parasitic effects, and apply techniques to manage gain-bandwidth trade-offs in analog systems

CO5: Design, analyse, and troubleshoot operational amplifiers and phase-locked loop circuits

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	-	3	3	2	-	3	2	-
CO2	3	-	3	3	2	-	3	2	-
CO3	3	-	3	3	2	-	3	3	-
CO4	3	-	3	3	3	2	3	3	-
CO5	3	2	3	3	3	3	3	3	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

The course builds foundational skills in analog circuit design, which is essential for innovation in electronics, communication, medical devices, transportation, and industrial automation.

Students gain the ability to design efficient, reliable, and high-erformance integrated circuits, which are critical components in sustainable technological infrastructure.

ECF 6223	EMBEDDED LINUX	L	T	P	C
SDG: 4,9		2	0	2	3

COURSE OBJECTIVES:

COB1: Explain the foundational principles of Linux and its relevance to embedded system design.

COB2: Describe the configuration, compilation, and booting processes of embedded Linux systems using appropriate toolchains and bootloaders.

COB3: Describe the process of developing device drivers in an embedded Linux environment.

COB4: Illustrate the application of hardware emulation tools such as QEMU in embedded Linux development.

COB5: Develop customized embedded Linux images using Yocto frameworks

MODULE I LINUX FUNDAMENTALS L:8 T: 0 P:8

Linux Community - Desktop vs Embedded - Desktop Linux - Different Linux flavors - Basic Linux Commands - Embedded Linux Basics - Architecture - Hardware Interfaces Supported - Development languages and tool - Host target development setup - Real-time Linux

MODULE II KERNEL INITIALIZATION & DEVICE HANDLING L:7 T:0 P:8

Embedded Linux Kernel Overview - Kernel Configuration - Compiling The Kernel - Communication between kernel and user space - The Linux Boot Process - The Root File system – Boot loaders In Embedded Linux - Porting Of Linux

MODULE III LINUX DRIVERS & HARDWARE EMULATORS L:8 T:0 P:8

Introduction to device drivers - Basic components of device drivers - Understandings Needed To Develop A Device Driver - Structure Of Device Driver - __init and __exit attributes - Hardware emulator – QEMU

MODULE IV BUILDING CUSTOM LINUX IMAGE - YOCTO L:7 T:0 P:6

Building Custom Linux Images - Yocto Project - Poky Distribution - Bitbake and commands -Recipes - meta-Layers - Build directory - Adding Layers and Image configurations - Adding Custom application on Core Image Minimal Build.

PRACTICALS

1. To install a virtual box and add Ubuntu 18 OS to the virtual box hosted on a windows machine.
2. To flash the Raspbian image into the SD card and boot the raspberry pi 4 -
    a. Execute the Linux commands for the file system
    b. Execute the Linux command to see the running process in raspberry pi
    c. Execute the Linux command to see the eMMC partition utilization on raspberry pi
3. Develop a Linux device driver for any simple module of your interest and add it to the raspberry pi file system
4. Using the git command fetch the yocto build environment for NXP i.Mx 8 on the ubuntumachine.
5. Write a hello_world.cpp, add it to the environment, build a core-image minimal and visualize the output using QEMU

L – 30; P – 30; Total Hours:60

TEXT BOOKS:

1. KarimYaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, “Building Embedded linux systems”, O'Reilly, 2008.
2. P. Raghavan, Amol Lad, SriramNeelakandan, “Embedded Linux System Design and Development”,Auerbach Publications, Taylor and Francis, 2006.
3. Craig Hollabaugh, “Embedded Linux : Hardware, Software, and Interfacing” Addison-Wesley, 2002.

REFERENCES:

1. KarimYaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates,2008 i.MX Yocto Project User's Guide - Rev. LF5.15.32_2.0.0 — 12 July 2022.

COURSE OUTCOMES:

CO1: Explain the structure of Linux OS, the architecture of embedded Linux, and basic Linux command usage.

CO2: Illustrate and apply the process of configuring, building, and booting embedded Linux systems

CO3: Analyze kernel and driver components, and describe their interaction within an embedded system

CO4: Evaluate hardware emulators and construct custom embedded Linux images using Yocto

CO5: Design and develop custom applications tailored for embedded Linux environments.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	2	2	1	3	2	1
CO2	2	1	3	3	3	2	3	3	2
CO3	3	1	3	3	3	2	3	3	2
CO4	2	1	3	2	2	3	2	3	2
CO5	3	2	3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Real-time operating system knowledge will provide useful information for high-quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement: able to advance industrialization through the use of real-time operating system concepts.

ECF 6224	EMBEDDED SYSTEMS LABORATORY	L	T	P	C
SDG: 4,8,9		0	0	2	1

COURSE OBJECTIVES:

COB1: To identify the software tools used in design of embedded systems with ARM processors.

COB2: To develop programming skills in design of ARM based embedded systems

COB3: To interface peripherals with ARM Processors.

COB4: To understand the importance of multitasking and scheduling in RTOS.

COB5: To implement an Embedded system.

PRACTICALS **L:0 T: 0 P:30**

List of Experiments

1. I\O Programming with ARM Processors.
2. Design with ARM Processors: ADC, DAC.
3. Timer Programming with ARM Processors.
4. Serial port Programming with ARM Processors.
5. Interrupt Programming with ARM Processors.
6. Interfacing LCD with ARM Processors.
7. Stepper motor interfacing with ARM Processors.
8. Multitasking in Real time Operating system(RTOS).
9. Scheduling in Real time Operating system(RTOS).
10. Interfacing sensors with SoC.
11. Interfacing Actuators with SoC.
12. Mini project

P – 30; Total Hours:30

TEXT BOOKS:

1. Andrew N. Sloss, DonimicSymes, Chris Wright, ARM System Developer's Guide
2. SteaveFurber, ARM system - on - chip architecture, Addison Wesley, 2000
3. Joseph Yiu, The Definitive Guide to the ARM Cortex-M3, 2nd edition. Netherlands: Newnes, 2009

REFERENCES:

1. Shibu.K.V, “Introduction to Embedded Systems”, TataMcgraw Hill,2009
2. Lyla B Das,” Embedded Systems-An Integrated Approach”,Pearson 2013
3. Tammy Noergaard, ”Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006
4. JonathanW.Valvano,”Embedded Microcomputer Systems,Real Time Interfacing”,Cengage Learning,3rd edition,2012.

COURSE OUTCOMES:

CO1: Simulate simple application programs through Keil µ vision.

CO2: Interface I/O ports and timers with ARM Microcontrollers

CO3: Appreciate the use of multitasking techniques in real timesystems, understand the fundamental concepts of real-time operating systems

CO4: Program in SoC using Python Language

CO5: Enrich their knowledge with hands on experiments and project based learning

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	3	3	3	-	-	3	2	-
CO2	2	2	2	3	2	-	3	3	-
CO3	2	2	2		3	-	3	3	2
CO4	3	2	2	2	3	-	2	3	2
CO5	2	3	3	3	3	2	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement:

Understanding of the Embedded Lab course will bring a global impact on quality education.

SDG 8: Development of new technologies provides sustainable economic growth and productive employment.

Statement: Design of new technologies based on Embedded System promotes sustained economic growth.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement: Able to apply the design concepts of Embedded systems to promote industrialization.

ENF 6281	PROFESSIONAL COMMUNICATION	L	T	P	C
SDG: 4 & 8		0	0	2	1

COURSE OBJECTIVES:

COB1: To introduce the fundamentals of professional communication in workplace contexts.

COB2: To develop structured presentation and public speaking skills.

COB3: To develop students' proficiency in written correspondence, including emails, and reports.

COB4: To enhance awareness and use of body language in professional settings

COB5: To instil appropriate workplace etiquette and digital professionalism.

MODULE I COMMUNICATION AT THE WORKPLACE P: 6

Language and communication fundamentals, Types of workplace communication, Formal and informal Communication, Direction and flow of communication- Organizational communication and interpersonal dynamics, 7 Cs of Communication - Ethical use of AI assisted communication tools

MODULE II PRESENTATION & PUBLIC SPEAKING SKILLS P: 6

Importance of presentation skills, Managing public speaking anxiety, Structured planning and delivery of presentations, Use of visual aids and technology - Interactive tools

MODULE III CORRESPONDENCE AT WORK P: 9

Digital correspondence - Email Writing and Etiquette, Report Writing: Incident Reports, Feasibility Reports, and Executive Summaries

MODULE IV BODY LANGUAGE P: 5

Fundamentals of body language in professional communication, Types of non-verbal cues, posture -Interpreting and responding to non-verbal signals in interpersonal and group contexts, Cultural variations in body language and their implications in global communication

MODULE V WORKPLACE ETIQUETTE P: 4

Workplace etiquette, Cultural sensitivity in globalized work environments, Gender sensitivity and inclusivity, DEI, Netiquette and digital professionalism - video conferencing, Professional networking (Social media, LinkedIn, etc.), Virtual team dynamics

P – 30; Total Hours:30

TEXT BOOKS:

1. Course material by the Department of English

REFERENCES:

3. Bovee, C. L., & Thill, J. V. *Business Communication Today* (14th ed.). Pearson, 2021.
4. Cardon, P. W., & Marshall, B. The hype and reality of social media use for work collaboration and team communication. *International Journal of Business Communication*, 52(3), 2015, 273–293.
5. Guffey, M. E., & Loewy, D. *Essentials of Business Communication* (11th ed.). Cengage Learning, 2020.
6. Jones, D. A., & Pittman, M. The digital professionalism paradox: Workplace norms and expectations in the era of online communication. *Journal of Applied Communication Research*, 49(3), 2021, 283–301.
7. Keyton, J., & Smith, F. L. M. Communication practices of work teams: Task, social, and identity functions. *Journal of Business Communication*, 46(4), 2009, 402–426.
8. Krizan, A. C., Merrier, P., Logan, J., & Williams, K. *Business Communication* (9th ed.). Cengage Learning, 2016.
9. Lesikar, R. V., Flatley, M. E., Rentz, K., & Lentz, P. *Lesikar's Business Communication: Connecting in a Digital World* (13th ed.). McGraw-Hill Education, 2019.
10. Madlock, P. E. The link between leadership style, communicator competence, and employee satisfaction. *Journal of Business Communication*, 45(1), 2008, 61–78.
11. Raman, M., & Sharma, S. Technical communication: Principles and practice (3rd ed.). Oxford University Press, 2015.
12. Robles, M. M. Executive perceptions of the top 10 soft skills needed in today's workplace. *Business Communication Quarterly*, 75(4), 2012, 453–465. https://doi.org/10.1177/1080569912460400

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: Demonstrate clarity in professional communication by selecting appropriate modes and formats for workplace interactions.

CO2: Deliver structured presentations with confidence, using relevant verbal and visual communication techniques.

CO3: Produce clear and effective written correspondence, including emails, and formal reports.

CO4: Interpret and apply non-verbal communication cues appropriately in professional contexts.

CO5: Exhibit workplace etiquette, digital conduct, and cultural sensitivity in professional environments.

Board of Studies (BoS):

18th BoS of the Department of English held on 04.06.2025

Academic Council:

24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4
CO1	2	3	2	2
CO2	2	3	2	2
CO3	2	3	-	-
CO4	2	3	2	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all

Statement: This course ensures that the students acquire quality education and are also made eligible to obtain productive and decent employment.

SDG 8: Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all

Statement: This course equips students with the competencies required for employment in a dynamic global workforce.

ECF 6225	MINI PROJECT	L	T	P	C
SDG: 4		0	0	6	3

COURSE OBJECTIVES:

COB1: Enhance professional competency and foster a strong research attitude.

COB2: Apply design principles and techniques to prototype development and modeling in VLSI and Embedded domain.

COB3: Develop technical skill sets aligned with the requirements of core industries.

COB4: Acquire proficiency in preparing technical reports and documentation.

COB5: Demonstrate the ability to work effectively in teams and manage projects in multidisciplinary environments.

GUIDELINES **L:0 T: 0 P:90**

1. Mini Project work can be a design project/experimental project in VLSI and Embedded Systems.
2. The project work is allotted individually to students.
3. The students shall be encouraged to do their project work in the institute itself. If found essential (Industry oriented Projects), they may be permitted to continue their project outside the institute. In such cases, the mini project work shall be jointly supervised by a faculty of the Department and the faculty of the other department of the University or an Engineer / Scientist from other reputed organization. The student shall meet the faculty periodically and attend the periodic reviews for evaluating the progress.
4. Department will constitute an Evaluation Committee to review the project work.
5. The Evaluation committee consists of subject experts, internal supervisor and experts in the specified area of the project.
6. Project evaluation consists of thesis work, two reviews of the work and the submission of project report with the viva voce.

7. First review would highlight the topic, objectives, methodology and expected results.
8. Second review evaluates the progress of the work, draft of the project report and demo of the prototype model.
9. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

L – 0; T – 0; P – 90; Total Hours:90

COURSE OUTCOMES:

CO1: Formulate and define a relevant technical problem based on literature or industrial need in VLSI/Embedded domain.

CO2: Apply appropriate tools, techniques, and knowledge to design or simulate a viable solution.

CO3: Apply theoretical and practical knowledge to identify and solve real-time engineering problems.

CO4: Design and implement cost-effective and efficient project ideas addressing practical needs.

CO5: Demonstrate subject knowledge through the development and evaluation of prototype models.

Board of Studies (BoS):
27th BOS of Department of ECE held on 26.06.2025

Academic Council:
24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO 6	PSO 1	PSO2	PSO3
CO 1	H	M	M	H	–	–	H	M	–
CO 2	H	H	H	H	M	–	H	H	–
CO 3	H	H	M	–	H	–	H	H	M
CO 4	M	M	L	M	H	–	M	H	M
CO 5	M	M	H	H	H	M	H	H	H

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Focuses on design thinking, optimization a critical problem-solving skill, and relates to sustainable development principles.

SEMESTER III

ECF 7121	**MIXED SIGNAL INTEGRATED CIRCUIT**	**L**	**T**	**P**	**C**
SDG: 9		**3**	**0**	**0**	**3**

COURSE OBJECTIVES:

COB1: Understand the necessity of mixed signal systems

COB2: Analyse Op-Amp to meet the mixed signal specifications.

COB3: Design CMOS comparators to meet the high-speed requirements of digital circuitry.

COB4: Develop efficient data converter circuits for mixed signal systems

COB5: Familiar with mixed signal processing circuits

MODULE I SAMPLING L:9 T:0 P:9

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

MODULE II SAMPLE-AND-HOLD CIRCUITS L:9 T:0 P:9

Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, effect of offset and application of switched capacitor circuits to minimize offset errors, Parasitic affects.

MODULE III SWITCHED CAPACITOR CIRCUITS L: 9 T:0 P:9

Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic Insensitive Integrators, Signal-Flow-Graph Analysis. Design of filters based on switched capacitor circuits,

MODULE IV COMPARATORS L: 9 T: 0 P:9

Ideal comparator, practical model of comparator, resolving capability, propagation delay, small signal analysis, conditions for slewing, evaluation of propagation delay for single pole and two pole comparators, Design of Linear response comparators, slew-rate limited

comparators, comparators with positive feedback, analysis of latched Comparators, Architecture of High-speed comparators, self-biased comparators, push pull comparators.

MODULE V DATA CONVERTERS L: 9 T: 0 P:9

Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity Integrating Converters, Design of Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Principles of Sigma-Delta ADC, Testing of data converters.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. BehzadRazavi, Design of Analog CMOS Integrated Circuits" McGraw Hill Education, 2017, 2nd Edition.
3. R. Jacob Baker, CMOS: Mixed-Signal Circuit Design, Wiley, 2008, 2nd Edition

REFERENCES:

1. Rui Paulo da Silva Martins and Pui-In Mak, "Analog and Mixed-Signal Circuits in Nanoscale CMOS", Springer, 2024
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.
3. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

COURSE OUTCOMES:

COB1: Understand and analyze the principles of signal sampling, including spectral properties, oversampling techniques, and error analysis in time-interleaved systems.

COB2: Apply circuit-level knowledge to design and test CMOS sample-and-hold circuits while minimizing charge-injection and offset-related errors using switched capacitor techniques.

COB3: Design and evaluate switched capacitor circuits for analog signal processing, including the development of filters and parasitic-insensitive integrators.

COB4: Analyze the operation and performance metrics of various types of comparators and design comparator architectures for high-speed and precision applications.

COB5: Examine and design digital-to-analog and analog-to-digital data converters, understand performance limitations, and implement testing strategies for accuracy and linearity.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1		2	3	3			3		1
CO2		2	3	3			3	3	1
CO3		1	3	3			3	3	2
CO4		3	3		3		3	3	2
CO5	2	3	3	3		3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

The course deals with advanced analog and mixed-signal circuit design (e.g., sample-and-hold circuits, switched capacitor circuits, comparators, and data converters), which are essential components in modern electronic systems that drive innovation in industries like healthcare, automotive, and communication.

ECF 7122	INDUSTRY INTERNSHIP	L	T	P	C
SDG: 4		0	0	4	2

COURSE OBJECTIVE:

COB1: Apply theoretical knowledge of VLSI design and embedded systems principles to real-world industrial projects.

COB2: Utilize Electronic Design Automation (EDA) software for the design, simulation, and testing of integrated circuits (ICs) and embedded systems hardware/software frameworks.

COB3: Analyze and debug complex systems by integrating hardware and software components, employing practical skills.

COB4: Collaborate effectively within a professional team environment, applying organizational policies and demonstrating communication, project management, and ethical conduct skills

COB5: Develop problem-solving and critical thinking skills by addressing industry-specific challenges in the VLSI and embedded systems domain

COURSE DESCRIPTION:

1. To earn credits for this course, industrial training for a period of 30 days, in a single slot, is mandatory. The course has to be undertaken during the first year summer vacation and the credits will be awarded in the third semester.
2. If the student is not able to complete the internship during the first year summer vacation, he/she can complete the course in a single slot in 3rd semester vacation.
3. For effective implementation of the course Industry Internship, a teaching faculty is appointed as the coordinator by the Head of the department.
4. The students will be allowed to undergo training only in reputed companies/research labs/design centers.

5. Interacting with the respective industries, where the students do their internship, the Coordinator continuously monitors the performance of the students during the internship.

6. After completion of the internship, the students are required to submit a detailed report and present what they had learned. The students should submit the industry certificate at the time of giving the presentation.

7. The performance of the student will be evaluated by the industry as well as the institute. Both the evaluations will be considered and aggregated to award the final grade. 50% weightage is given to the evaluation by the industry and remaining 50% weightage to the evaluation by the committee appointed by the Head of the Department.

COURSE OUTCOMES:

At the end of the internship, the student will be able to:

CO1: Solve problems typically encountered by engineers in industry.

CO2: Identify and address social, economic, and safety issues in an engineering problem and develop a solution that addresses this.

CO3: Learn new concepts and apply them to the solution of engineering problems.

CO4: Function effectively on a multidisciplinary team and with other areas of the organization.

CO5: Clearly communicate their ideas orally and in writing.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	2	2	2	3	2	2	2	2
CO2	2	2	2	2	2	2	2	2	2
CO3	2	2	2	2	2	2	2	2	2
CO4	2	2	2	2	2	2	2	3	3
CO5	2	2	2	2	3	3	2	3	3

*** Legend: L – Low (1), M – Medium (2), H – High (3)**

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Focuses on gaining training, skill set and industry exposure in VLSI and Embedded Companies for one’s own sustainable development.

ECF 7123	**Project Work– Phase I (III Sem)**	**L**	**T**	**P**	**C**
		0	**0**	**14**	**7***
ECF 7123	**Project Work– Phase II (IV Sem)**	**L**	**T**	**P**	**C**
SDG:4		**0**	**0**	**35**	**18**

COURSE OBJECTIVES:

COB1: To enable students to undertake independent research or development work relevant to VLSI and Embedded System Design.

COB2: To apply advanced knowledge, techniques, and tools in solving real-world or research problems.

COB3: To enhance project planning, execution, and management skills.

COB4: To develop skills in technical documentation and effective communication.

COB5: To cultivate innovation, ethical practice, and lifelong learning in professional work.

COURSE DESCRIPTION

Project work shall be carried out by each and every individual student under the supervision of a faculty of this department. A student may however, in certain cases, be permitted to work for the project in association with other departments or in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and the faculty of the other department of the University or an Engineer / Scientist from the organization. The student shall meet the faculty periodically and attend the periodic reviews for evaluating the progress.

There will be three reviews for continuous assessment and one final review and viva voce at the end of the semesters. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department. The research findings have to be published in conference/Journal.

COURSE OUTCOMES:

At the end of the project work, the student will be able to:

CO1: Design and implement a complete VLSI and/or embedded system for a specific application, applying knowledge of design principles, methodologies, and industry practices.

CO2: Utilize modern Electronic Design Automation (EDA) tools and software to design, analyze, and verify complex integrated circuits and embedded systems.

CO3: Analyze and optimize the performance of VLSI and embedded systems with consideration for key design trade-offs, including power dissipation, speed (timing analysis), area, and testability.

CO4: Independently conduct research and investigation to identify, formulate, and solve practical engineering problems within the VLSI and embedded systems domain, proposing innovative and optimal solutions

CO5: Manage a project effectively, which includes developing a project proposal, planning, and documentation, while adhering to professional and ethical standards.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	1	-	2	3	1	1	3	-	-
CO2	-	-	1	-	3	1	-	3	-
CO3	-	-	1	-	-	1	-	-	-
CO4	3	-	1	-	-	1	-	1	-
CO5	1	3	1	-	1	2	-	2	3

* Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Focuses on novel design, its development and employability and relate to sustainable development principles.

MOOC	L	T	P	C
	0	0	0	0

GENERAL GUIDELINES:

1. Students shall identify a MOOC course related to his/her project topic in consultation with the project supervisor.
2. Student shall register for a MOOC course with minimum two credit offered by any recognized organization during the project phase I.
3. Selection and completion of MOOC course by the students shall be endorsed by Head of the Department.

PROFESSIONAL ELECTIVE COURSES

ECFY 001	LOW POWER IC DESIGN	L	T	P	C
SDG: 7,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Learn what causes power loss in CMOS and MOSFET circuits used in VLSI design.

COB2: Find ways to reduce power loss in circuits by using proper transistor sizing and logic techniques.

COB3: Use methods to save power in system parts like clock signals, buses, and memory.

COB4: Analyze and measure how much power is used in circuits using models and data.

COB5: Apply software-related techniques and co-design methods to reduce power in embedded systems.

MODULE I POWER DISSIPATION IN CMOS L:9 T: 0 P:0

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET , gate induced drain leakage– Power dissipation in CMOS : short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit, device limit, system limit.

MODULE II DESIGN OF LOW POWER CIRCUITS L:9 T: 0 P:0

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing, Varieties of Boolean Functions, Adjustable Device Threshold Voltage.

MODULE III POWER OPTIMIZATION USING SPECIAL TECHNIQUES **L:9 T: 0 P:0**

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Word line and Reduced bit line Swing.

MODULE IV POWER ESTIMATION **L:9 T: 0 P:0**

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power Sensitivity Analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach, steepest descent, generic based algorithm based approach.

MODULE V SOFTWARE DESIGN FOR LOW POWER **L:9 T: 0 P:0**

Sources of software power dissipation - software power estimation: Gate level, architecture level, bus switching activity, instruction level power analysis - software power optimization: minimizing memory access costs, instruction selection and ordering, power management - Automated low power code generation – Co-design for low power.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2009.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998

REFERENCES:

1. DimitriosSoudris, Christians Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002

2. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing Ashok N Kamthane, “Computer Programming”, Pearson Education, 2nd Edition, India, 2012. (ISBN 13: 9788131704370)
3. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001

COURSE OUTCOMES:

CO1 Explain how power is lost in CMOS circuits and what limits power reduction.

CO2 Design low power circuits using proper sizing and special flip-flops.

CO3 Describe the clock, memory, and bus techniques to save system power.

CO4 Estimate power consumption using modelling, signal analysis, and algorithmic methods.

CO5 Apply software-level power-saving strategies in hardware–software co-design.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	2	2	3	-	2	2	-
CO2	3	-	3	3	2	2	3	3	2
CO3	2	-	2	2	3	2	3	2	2
CO4	3	3	3	3	3	3	3	3	3
CO5	3	3	3	3	3	3	2	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 7: Affordable and Clean Energy

Ensure access to affordable, reliable, sustainable, and modern energy for all.

Low power VLSI design directly reduces energy consumption in electronic devices and embedded systems. By designing energy-efficient circuits, the course contributes to reducing global energy demand and promoting sustainable energy use.

SDG 9: Industry, Innovation, and Infrastructure
Build resilient infrastructure, promote inclusive and sustainable industrialization, and foster innovation.

This course empowers students to innovate in semiconductor technology and embedded systems. It enhances their ability to design energy-efficient solutions, fostering industrial competitiveness and sustainable tech development.

ECFY 002	ASIC DESIGN	L	T	P	C
SDG: 4		3	0	0	3

COURSE OBJECTIVES:

COB1: Explain the design flow of different types of ASIC.

COB2: Classify various programming technologies and logic devices used in ASIC implementation.

COB3: Compare the architectures and characteristics of different types of programmable ASICs.

COB4: Summarize the key components and design methodologies of System-on-Chip (SoC) architectures.

COB5: Analyze techniques for power reduction and efficient on-chip communication in modern VLSI systems.

PREREQUISITES

VLSI Design Flow, IC layout

MODULE I ASIC DESIGN FLOW AND PROGRAMMABLE ASIC 9

Types of ASICs – Full custom ASIC- Standard cell based ASIC- Gate array based ASIC- Programmable logic devices architecture - ASIC Design flow – CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell.

MODULE II PROGRAMMABLE ASICs AND LOGIC CELLS 9

Programming technology-Antifuse - static RAM - EPROM and EEPROM technology - PREP benchmarks, Programmable ASIC logic cells-Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX , Programmable interconnects, Programmable ASIC I/O cells-DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III ASIC PHYSICAL DESIGN 9

System partitioning – partitioning methods –Algorithms. Floor planning – measurement of delay-floor planning tools- I/O, power and clock planning. placement – means of placement goals and objectives –placement algorithm. Routing: global routing – detailed routing.

MODULE IV INTRODUCTION TO SOC 9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures-characteristics-data transfer modes, On-Chip Communication Architecture Standards, AMBA 2.0-AHPB- Advanced peripheral bus-AMBA 3.0

MODULE V SYNTHESIS OF ON-CHIP COMMUNICATION ARCHITECTURES AND TECHNIQUES FOR POWER REDUCTION 9

Bus Topology Synthesis- Hierarchical Bus Architecture Topology Synthesis –Bus Matrix Topology Synthesis- Bus Protocol Parameter Synthesis -Component Mapping -Arbitration Scheme Synthesis-Full AMBA bus matrix architecture- Techniques for Power Reduction- Techniques for Reducing capacitive crosstalk delay and capacitive crosstalk effects.

L – 45; TOTAL HOURS –45

TEXT BOOKS:

1. M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson, 2003
2. Sudeep Pasricha and NikilDutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsevier, 2008

REFERENCES:

1. H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.
2. J. M. Rabaey, A. Chandrakasan, and B. Nikolic,” Digital Integrated Circuit Design Perspective (2/e)”, PHI 2003.
3.Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, “Low-Power NoC for High Performance SoC Design”, CRC Press, 2008.

COURSE OUTCOMES:

CO1: Describe the VLSI design flow and analyse the architecture of FPGAs.

CO2: Design logic devices using various programming technologies.

CO3: Illustrate programmable ASIC architectures and implement logic functions using different logic cells.

CO4: Explain System-on-Chip design principles and evaluate on-chip communication protocols such as AMBA and AXI using platform-based design.

CO5: Apply synthesis strategies and evaluate power optimization techniques in VLSI design.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	1	2	3	2	2	1	3	3	2
CO2	2	1	3	3	3	2	3	3	2
CO3	2	2	3	3	3	2	3	3	2
CO4	2	2	3	3	3	2	2	3	2
CO5	2	2	3	3	3	3	2	3	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Quality Education.

Statement: It is a elective course that explains the VLSI CAD flow which intend to provide quality education

ECFY 003	TESTING OF VLSI CIRCUITS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Extend automated and manual techniques for generating tests for faults in digital circuits and systems

COB2: Show the generation of test vectors for combinational and sequential circuits

COB3: Develop built-in self-test patterns.

COB4: Classify Crosstalk fault effects and test pattern generation

COB5: Classify Testing of algorithms for digital circuits.

PREREQUISITES: VLSI Design, Fault models

MODULE I INTRODUCTION TO VLSI TESTING AND FAULT MODELLING **L:9 T:0 P:0**

Introduction to VLSI testing- Importance of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing. Fault Types, Functional Vs Structural Testing, Levels of Fault Models, Fault Equivalence, Equivalence of Single Stuck-at Faults, Fault Collapsing, Fault Dominance. Logic & Fault Simulation, Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation &Fault Simulation. SCOAP –Combinational controllability and observability.

MODULE II COMBINATIONAL AND SEQUENTIAL TEST GENERATION **L:9 T:0 P:0**

Combinational Circuit Test Generation-Algorithms and Representations, Structural vs. Functional Test, Automatic Test-Pattern Generator, Search Space Abstractions, Algorithm Completeness, ATPG Algebras, Algorithm Types, Redundancy Identification (RID), Significant Combinational ATPG Algorithms- D-Calculus and D-Algorithm (Roth), PODEM. Sequential Circuit Test Generation- ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Cycle-Free Circuits, Cyclic Circuits.

MODULE III MEMORY TESTING AND DESIGN FOR TESTABILITY **L:9 T:0 P:0**

Functional RAM testing, testing RAM neighborhood pattern - sensitive faults and layout related faults, cache RAM chip testing, ROM chip testing, memory built-in self-test, design for testability basics -ad hoc approach, and structured approach. Scan Cell Designs - Scan Architectures, Full-Scan Design, Muxed-D Full-Scan Design, Clocked Full-Scan Design, LSSD, Partial-Scan Design, Scan Design Rules, Scan Design Flow, Special-Purpose Scan Designs, RTL Design for Testability.

MODULE IV BUILT-IN SELF-TEST L:9 T:0 P:0

Built-in Self-Test Design rules -Test Pattern Generation for BIST-Exhaustive Testing – Exhaustive testing-Pseudo-random testing- Delay fault Testing - Output Response Analysis -Transition Count- Signature Analysis -BIST Architectures -Built-in Logic Block Observer- Modified Built-in Logic Block Observer -circular self test path.

MODULE V BOUNDARY SCAN, ANALOG AND SYSTEM TESTING L:9 T:0 P:0

System configuration with Boundary Scan, Analog testing - Analog circuit design for testability, Analog Test Bus, functional test ,Diagnostic test.

L – 45; Total Hours:45

TEXT BOOKS:

1. Parag K. Lala, “An Introduction to Logic Circuit Testing”, Texas A&M University–Texarkana, 2009.

2. Angela kristic, “Delay fault testing for VLSI circuits”, Springer science, 2013.

3. S.Jayanthy, MC Bhuvaneshwari, “Test generation of cross talk delay faults in VLSI circuits”, Springer, 2019.

REFERENCES:

1. Bushnell and Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits”, Kluwer Academic Publishers, 2002

2. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.

3. Laung-Terng Wang , Cheng-Wen Wu , Xiaoqing Wen , Khader and S. Abdel-Hafez ,”VLSI Test Principles and Architectures: Design for Testability”, Morgan Kaufmann; 1st edition, 2006.

COURSE OUTCOMES:

On completion of the course, students will be able to

COB1: generate test vectors using stuck-at models for combinational circuits

COB2: model circuit with testability perspective

COB3: generate a test vector for sequential circuits

COB4: show the architecture of built-in self-test and fault diagnosis.

COB5: design the test pattern for cross-talk fault.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	3	3	3	2	3	3	2
CO2	2	2	3	3	3	3	3	3	2
CO3	3	1	3	3	3	2	3	3	2
CO4	2	2	2	2	3	2	2	3	2
CO5	2	1	3	3	3	2	3	2	1

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Quality Education – This course empowers students with contemporary RFIC design knowledge relevant to academic and industrial research.

Statement: providing students with essential knowledge and practical skills in VLSI testing, enabling them to understand fault modelling, test generation, and design-for-testability, thereby promoting quality education in semiconductor design and reliability engineering.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement: Equipping students with skills to design and implement reliable and fault-resilient VLSI systems, fostering innovation in semiconductor testing technologies and promoting sustainable industrial practices through efficient and cost-effective testing methodologies.

ECFY 004	SCRIPTING LANGUAGES FOR VLSI	L	T	P	C
SDG: 4,9	DESIGN AUTOMATION	3	0	0	3

COURSE OBJECTIVES:

COB1: To introduce the fundamentals of PERL programming, including scalar data, arrays, hashes, and control structures.

COB2: To develop proficiency in advanced PERL concepts such as file handling, directory operations, and modular programming.

COB3: To provide a foundational understanding of the TCL language and its syntax, control flow, and error handling.

COB4: To expose students to advanced TCL programming with a focus on file access, process control, and GUI basics using Tk.

COB5: To familiarize students with Universal Verification Methodology (UVM) and its components for developing verification environments.

MODULE I PERL BASICS L:9 T: 0 P:0

History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.

MODULE II ADVANCED PERL L:9 T: 0 P:0

Directory access - File and Directory manipulation - Process Management - Packages and Modules.

MODULE III TCL BASICS L:9 T: 0 P:0

An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow – procedures - Errors and exceptions - String manipulations.

MODULE IV ADVANCED TCL L:9 T: 0 P:0

Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.

MODULE V UNIVERSAL VERIFICATION METHODOLOGY L:9 T: 0 P:0

Introduction to UVM - Verification components - Transaction level modelling – Developing.

L – 45; Total Hours:45

TEXT BOOKS:

1. Schwartz, Randal L., and Tom Phoenix. Learning perl. " O'Reilly Media, Inc.", 2021.
2. Hall, Joseph N. "Effective Perl programming." ; login:: the magazine of USENIX & SAGE 24, no. 3 2020: 53-57.
3. Saltzman, Michael. Modern Perl Programming. Prentice Hall Professional Technical Reference, 2020.
4. Orwant, Jon. Games, Diversions & Perl Culture: Best of the Perl Journal. " O'Reilly Media, Inc.", 2003.
5. Wall, Larry. "Tom Christiansen, and Jon Orwant." Programming Perl (2000): 558-568.

REFERENCES:

1. Vanessa R. Copper, “Getting started with UVM: A Beginner’s Guide”, Verilab Publishing, First Edition, 2013.
2. Salemi, Ray. The UVM primer: An introduction to the universal verification methodology. Boston Light Press, 2013.
3. Wright, John Charles. Physically aware design of generated systems-on-chip. University of California, Berkeley, 2021.
4. Spear, Chris. SystemVerilog for verification: a guide to learning the testbench language features. Springer Science & Business Media, 2008.

COURSE OUTCOMES:

COB1: Demonstrate the use of basic PERL constructs such as variables, arrays, hashes, and regular expressions in program development.

COB2: Implement advanced PERL functionalities including file and directory operations, process control, and modular design.

COB3: Develop and debug basic TCL scripts using control statements, procedures, and list handling techniques.

COB4: Design TCL applications incorporating file and process management and simple graphical interfaces using Tk.

COB5: Apply the principles of Universal Verification Methodology to build and simulate efficient testbenches and verification components.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2		2	3	2		3	2	
CO2	3		3	3	2		3	3	
CO3	2		2	2	-		2	2	
CO4	2		2	3	2		2	2	
CO5	3	2	3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Quality Education – This course empowers students with contemporary RFIC design knowledge relevant to academic and industrial research.

Statement: providing students with essential knowledge and practical skills in VLSI testing, enabling them to understand fault modelling, test generation, and design-for-testability, thereby promoting quality education in semiconductor design and reliability engineering.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement: Equipping students with skills to design and implement reliable and fault-resilient VLSI systems, fostering innovation in semiconductor testing technologies and promoting sustainable industrial practices through efficient and cost-effective testing methodologies.

ECFY 005	RF INTEGRATED CIRCUIT DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To classify and compare various impedance matching techniques with modern tools and methods.

COB2: To design passive and active RF components in ICs using advanced CMOS and SOI technologies.

COB3: To simulate and evaluate amplifiers, oscillators, mixers and synthesizers with real-time specifications.

COB4: To analyze the effect of noise and distortion in RF design and apply modern noise reduction strategies.

COB5: To evaluate and construct practical transceiver architectures for current wireless standards (5G, WiFi6, UWB).

MODULE I IMPEDANCEMATCHINGANDAMPLIFIERS L:9 T: 0 P:0

Review of S-parameters and Smith Chart, Design of IC Passive Components for RF using EM Tools, Impedance Matching Networks: L, π, T, and Advanced Matching (LNA-focused),High-frequency amplifier design (Broadband LNAs, Narrowband LNAs),Power and Noise Matching Techniques, Differential and Single-ended LNAs, AGC-Controlled MOSFET Amplifier Design using Modern Simulation Tools (Cadence/AWR/ADS).

MODULE II FEEDBACKSYSTEMSANDPOWERAMPLIFIERS L:8 T: 0 P:0

Stability Analysis: Gain & Phase Margin, Nyquist and Bode Analysis Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, Power amplifiers- Power Amplifier Classes (Class A-F),Switching Power Amplifiers, Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MODULE III PLLANDFREQUENCYSYNTHESIZERS L:8 T: 0 P:0

Linear and Non-linear Modelling of PLLs, Phase Noise Considerations in Synthesizer Design, Phase Detectors, Loop Filters, Charge Pumps, Integer-N, Fractional-N

Synthesizers (Including Sigma-Delta PLLs). Direct Digital Synthesizers (DDS),Modern Frequency Synthesizer Architectures for 5G Transceivers.

MODULE IV MIXERSANDOSCILLATORS L:8 T: 0 P:0

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Tuned Oscillators, Cross-coupled. Resonator Design (MEMS/NEMS and SAW filters) Negative resistance oscillators, Phase Noise Modelling & Analysis.

MODULE V NOISEANDTRANSCEIVERARCHITECTURES L:12 T: 0 P:0

Noise: Thermal, shot, flicker, popcorn noise, and Modern Mitigation Techniques. Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver. Transmitter Architectures. Modern Radio Architectures: 5G NR, WiFi 6/6E, UWB, NB-IoT. Case Study: GSM, CDMA, LTE, and mm Wave Architectures.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. M. Steer, “Microwave and RF Design”, NC State University, 3rd Edition, 2019.
2. B. Razavi, “RF Microelectronics”, 3rd Edition, Wiley, 2022Saltzman, Michael. Modern Perl Programming. Prentice Hall Professional Technical Reference, 2020.

REFERENCES:

1. T.H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 3rd Edition, Cambridge University Press, 2021
2. B. Razavi, “Design of Analog CMOS Integrated Circuits”, 3rd Edition, McGraw-Hill, 2023.
3. SorinVoinigescu, “High-Frequency Integrated Circuits”, Cambridge University Press, 2nd Edition, 2019.

COURSE OUTCOMES:

COB1: Classify and compare various impedance matching techniques using modern RF tools.

COB2: Analyze and design low noise and power amplifiers using simulation tools.

COB3: Evaluate the performance of PLLs and frequency synthesizers and implement suitable solutions.

COB4: Design and analyze mixers and oscillators using CMOS technologies.

COB5: Develop and justify RF transceiver architectures for advanced wireless communication systems.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	1	1	3	3	3	3	3	3	-
CO2	3	1	3	3	3	3	3	3	1
CO3	3	1	3	3	3	-	3	3	3
CO4	3	1	3	3	3	-	3	3	1
CO5	3	3	3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement:
This course empowers students with contemporary RFIC design knowledge relevant to academic and industrial research.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:
Focus on emerging wireless technologies such as 5G, UWB and WiFi6/7 align with innovation-driven design.

ECFY 006	VLSI DIGITAL SIGNAL PROCESSING	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: Understand architectural techniques such as pipelining and parallel processing to improve the speed and efficiency of digital signal processing systems.

COB2: Build and optimize VLSI architectures for basic DSP algorithms

COB3: Interpret the VLSI design models in various domains of signal processing

COB4: Model the signal processing architectures for arithmetic operations

COB5: Explore fast convolution algorithms to develop high-speed DSP systems.

MODULE I PIPELINING AND PARALLEL PROCESSING L:10 T: 0 P:0

Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

MODULE II UNFOLDING L:7 T: 0 P:0

Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding.

MODULE III FOLDING L:8 T: 0 P:0

Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

MODULE IV SYSTOLIC ARCHITECTURE DESIGN L:10 T: 0 P:0

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

MODULE V FAST CONVOLUTION L:10 T: 0 P:0

Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

L – 45; T – 0; P – 0 Total Hours:45

TEXT BOOKS:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems: Design and Implementation, 2nd Edition, Wiley-Interscience, 2015.
2. Pramod Kumar Meher, “Arithmetic Circuits for DSP Applications”, Wiley IEEE press, 2017.
3. Hongjiang Song, ”Principles of VLSI Design - Symmetry, Structures and Methods”, Lulu Publishers, 2018.

REFERENCES:

1. U. Meyer – Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004

COURSE OUTCOMES:

CO1: Explain the concepts of pipelining and parallel processing, including retiming techniques for low-power VLSI DSP systems.

CO2: Apply unfolding algorithms to optimize digital signal processing architectures and reduce critical path delays.

CO3: Analyze folding transformations and evaluate register minimization techniques in folded and multirate DSP architectures.

CO4: Design systolic array architectures for applications such as FIR filtering and matrix multiplication using scheduling techniques.

CO5: Develop and evaluate fast convolution algorithms using Cook-Toom, Winograd, and cyclic convolution methods for efficient implementation.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3	3	2	2	3	2	
CO2			3	3	3		3	2	
CO3			3	3	2		3	2	
CO4			3	3	2	2	3	3	2
CO5			3	2			2	3	

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

To design efficient, low-power DSP systems using advanced VLSI techniques. It fosters innovation in digital hardware architecture crucial for sustainable technological advancement.

ECFY 007	QUANTUM COMPUTING	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To introduce fundamental concepts of quantum computation and information theory.

COB2: To understand the principles of quantum logic gates, circuits, and quantum algorithms.

COB3: To explore quantum error correction and fault tolerance mechanisms.

COB4: To study the architectural aspects and constraints in building quantum hardware.

COB5: To introduce to quantum technologies and quantum processors

MODULE I FUNDAMENTALS OF QUANTUM COMPUTING L:9 T: 0 P:0

Introduction, Classical vs. Quantum Computing, Qubits and Quantum States, Quantum Superposition and Entanglement, Postulates of Quantum Mechanics, Bloch Sphere Representation, Measurement of States.

MODULE II QUANTUM GATES AND CIRCUITS L:9 T: 0 P:0

Quantum Logic Gates: Pauli-X, Y, Z, Hadamard, Phase, T-Gate, Controlled Gates: CNOT, Toffoli, Fredkin, Quantum Circuits and Circuit Diagrams, Reversible Computing Basics.

MODULE III QUANTUM ALGORITHMS L:9 T: 0 P:0

Quantum Parallelism and Quantum Speedup, Deutsch-Jozsa Algorithm, Grover's Search Algorithm, Shor's Factoring Algorithm, Implications on Classical Cryptographic Hardware.

MODULE IV QUANTUM ERROR CORRECTION AND DECOHERENCE L:9 T: 0 P:0

Sources of Noise and Decoherence, No-Cloning Theorem, Quantum Error Correcting Codes (QECC), Shor Code, Steane Code, Fault Tolerant Quantum Computation.

MODULE V QUANTUM TECHNOLOGIES L:9 T: 0 P:0

Quantum Technologies: Superconducting Qubits, Ion Traps, Spin Qubits, Quantum Dot and Silicon-based Qubits, Integration of Quantum Circuits with CMOS, Cryogenic Requirements, Overview of Current Quantum Processors (IBM, Google, Intel, etc.)

L – 45; T – 0; P – 0 Total Hours:45

TEXT BOOKS:

1. Michael A. Nielsen, Isaac L. Chuang – *Quantum Computation and Quantum Information*, Cambridge University Press, 10th Anniversary Edition, 2010.
2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
3. Ray LaPierre, Introduction to Quantum Computing, Springer, 2021.

REFERENCES:

1. Phillip Kaye, Raymond Laflamme, Michele Mosca – *An Introduction to Quantum Computing*, Oxford University Press, 2007.
2. M. Hirvensalo – *Quantum Computing*, Springer, 3rd Edition, 2013.

COURSE OUTCOMES:

CO1: Understand and explain the foundational principles of quantum mechanics relevant to computing.

CO2: Design basic quantum circuits using standard gates and reversible logic.

CO3: Analyze quantum algorithms and compare their efficiency with classical counterparts.

CO4: Evaluate quantum error correction strategies and their impact on reliable quantum computation.

CO5: Explain different quantum technologies and understand how quantum processors are built and connected with CMOS circuits.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025	**Academic Council:** 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3				2		
CO2			3	3			3	3	
CO3	3		3		3			3	3
CO4	3		3	2	3		3	3	3
CO5			2	2		2	2	3	

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

Industry, Innovation and Infrastructure by helping students learn advanced quantum technologies that can lead to future innovations in computing and VLSI systems.

ECEY 008	EMBEDDED SYSTEM FOR ROBOTICS	L	T	P	C
SDG: 4, 8, 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To understand the selection and operation of sensors and actuators used in robotics and automation.

COB2: To analyze embedded control systems, multitasking, and communication protocols for robotic platforms.

COB3: To study robot kinematics and apply appropriate mathematical models for robotic manipulation.

COB4: To design mobile robot architectures and apply localization and navigation algorithms.

COB5: To explore embedded system applications of robotics in varied domains such as automotive, healthcare, and agriculture.

MODULE I SENSORS AND ACTUATORS FOR ROBOTIC APPLICATIONS **L:9 T: 0 P: 0**

Overview of sensor classification – Binary, Analog, Digital; Proximity Sensors – IR, Ultrasonic, and Capacitive; Motion sensors – Gyroscope, Accelerometer, IMU; Camera and LIDAR integration. Actuators: DC Motor, Stepper Motor, Servo Motor, Brushless DC Motor; Motor control techniques – H-Bridge, PWM. Interface circuits and signal conditioning.

MODULE II EMBEDDED CONTROL, MULTITASKING, AND COMMUNICATION **L:10 T: 0 P: 0**

Control algorithms – PID, Fuzzy Logic, Adaptive Control; Motor velocity and position control – Kinematics-to-control interface. Multitasking: RTOS concepts, Pre-emptive vs Cooperative Scheduling, Semaphores, Timer-Interrupts, Real-Time Task Scheduling. Communication: I2C, SPI, UART, CAN, BLE, and Wi-Fi; Fault tolerance in wireless robotic control.

MODULE III ROBOT KINEMATICS **L: 9 T: 0 P: 0**

Basic Concepts: Degrees of freedom, workspace, manipulators and end-effectors; Forward Kinematics using Denavit-Hartenberg parameters; Inverse Kinematics – closed-form and numerical solutions; Velocity Kinematics and Jacobian matrices; Kinematic singularities.

MODULE IV MOBILE ROBOT ARCHITECTURE AND LOCALIZATION ALGORITHMS **L: 9 T: 0 P: 0**

Locomotion Mechanisms: Wheeled, Tracked, Legged, and Aerial Robots; Omni-directional and Differential Drive Robots; Embedded platform selection – Microcontrollers, FPGAs, and SBCs. Localization and Navigation – Path and Maze Exploration – Map Generation using SLAM; Algorithms: A*, Dijkstra, Kalman Filter, Particle Filter.

MODULE V EMBEDDED SYSTEM APPLICATIONS IN ROBOTICS **L: 8 T: 0 P: 0**

Application-specific embedded system design for robots: Autonomous Vehicles – perception and embedded control; Warehouse Robots – localization and task automation; Agricultural Robots – environment sensing and smart actuation; Healthcare Robots – sensor integration, safety-critical embedded systems.

L – 45 ; T – 0 P – 0 ; Total Hours: 45

TEXT BOOKS:

1. Thomas Bräunl, “Embedded Robotics: Mobile Robot Design and Applications with Embedded Systems”, Springer Berlin Heidelberg, 2014, ISBN: 9783662050996
2. Nayan M., Kakoty, RupamGoswami and RamanaVinjamuri, “Introduction to Embedded Systems and Robotics”, Springer Nature Switzerland, 2024, ISBN: 9783031730986, 3031730984
3. NilanjanDey, Amartya Mukherjee, “Embedded Systems and Robotics with Open Source Tools” CRC Press, 2018, ISBN: 9781498734400, 1498734405.

REFERENCES:

1. R.K. Mittal and I.J. Nagrath, “Robotics and Control”, 3rd Edition, Tata McGraw-Hill, 2022.
2. John J. Craig, “Introduction to Robotics: Mechanics and Control”, 4th Edition, Pearson, 2021.
3. Morgan Quigley, Brian Gerkey, and William D. Smart, “Programming Robots with ROS”, O’Reilly, 2022.

COURSE OUTCOMES:

CO1: Select and integrate appropriate sensors and actuators in robotic systems.

CO2: Implement embedded control and multitasking strategies using modern communication protocols.

CO3: Apply kinematic principles for robotic manipulators and solve related models.

CO4: Design mobile robots and implement navigation algorithms for autonomous mobility.

CO5: Develop embedded robotic solutions for real-time applications in multiple domains.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	1	3	3
CO2	2	3	3	2	3	-	2	3	3
CO3	3	3	3	3	-	-	2	3	3
CO4	2	2	3	-	3	-	1	3	2
CO5	2	2	2	3	3	2	2	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all

Statement:

The course imparts interdisciplinary knowledge in embedded systems and robotics, enhancing students' technical proficiency and fostering lifelong learning essential for advanced problem-solving in real-world applications.

SDG 8: Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all

Statement:

By equipping learners with practical skills in automation, control, and intelligent robotic systems, the course supports the development of a future-ready workforce, contributing to productive employment in emerging technology sectors.

SDG 9: Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement:

The course enables students to design intelligent and resilient robotic systems using embedded technologies, which fosters innovation in automation and industrial applications, thereby contributing to sustainable and inclusive industrial development.

ECFY 009	EMBEDDED AUTOMOTIVE SYSTEMS	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To describe the automotive electronics

COB2: To utilize the automotive systems in automobiles.

COB3: To explore the new trends in automotive industry

COB4: To understand the applications of embedded systems in automotive industry.

COB5: To evaluate the impact of AUTOSAR on automotive embedded systems.

MODULE I ELECTRONICS IN THE AUTOMOBILE L:9 T: 0 P: 0

Introduction- Body and convenience electronics: vehicle power supply controllers and lighting modules, door control modules, Safety electronics: active safety systems: ABS, ASR, ESP, passive safety systems: Restraint systems and their associated sensors in an automobile. Power train Electronics: Gasoline engine management, Infotainment electronics: Dashboard/instrument cluster, car audio, telematics systems, navigation systems, multimedia systems.

MODULE II AUTOMOTIVE COMMUNICATION PROTOCOLS L:9 T: 0 P: 0

CAN bus - Concepts of bus access and arbitration - Error processing and management - Definitions of the CAN protocol: 'ISO 11898-1' - Errors: their intrinsic properties, detection and processing – Physical layer, Application layers for CAN – LIN - Basic concept of the LIN 2.0 protocol. FlexRay - Event-triggered and time-triggered aspects - TTCAN – Time-triggered communication on CAN- FlexRay

MODULE III AUTOMOTIVE EMBEDDED SYSTEMS L:9 T: 0 P: 0

Automotive Embedded systems. Microcontroller in Automobile applications - Different Types of Microcontrollers in Automotive systems – Challenges in ECU design - Growth in the Automobile – Application in Vehicle Control - Power train - Driver Information –ADAS

MODULE IV DRIVE BY WIRE L:9 T: 0 P: 0

Challenges and opportunities of X-by-wire: system & design requirements, steer-by-wire, brake- by-wire, suspension-by-wire, gas-by-wire, power-by-wire, shift by wire. Future of Automotive Electronics.

MODULE V AUTOSAR L:9 T: 0 P: 0

AUTOSAR Architecture- Basic concepts- Software components - Layered Architecture - Microcontroller Abstraction Layer – ECU Abstraction Layer - Complex Device Driver - Service Layer – RTE - Application Layer - Basic Software modules – Diagnostics - Methodology - Tools in SW development using Autosar

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2014
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, ArkadebGhosal, “Understanding and Using the Controller Area Network Communication Protocol “, Springer publishers,2012

REFERENCES:

1. Konrad Etschberger,”Controller Area Network: Basics, Protocols, Chips and Application”, IXXAT Press, 2001.
2. 2. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Embedded System Academy 2008.

COURSE OUTCOMES:

COB1: Design and develop embedded automotive systems.

COB2: Analyze various embedded products used in automotive industry.

COB3: Implement suitable communication protocols in automobiles.

COB4: Evaluate the opportunities involving technology, a product or a service required for developing an embedded automotive application.

COB5: Analyze the features of AUTOSAR Architecture.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	2	1	-	3	3	-
CO2	3	3	3	2	-	-	3	3	-
CO3	3	3	3	2	-	-	3	3	-
CO4	3	3	3	2	-	-	3	3	-
CO5	3	3	3	2	-	-	3	3	-

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

Enables reliable and efficient in-vehicle communication, critical for smart and autonomous vehicles.

ECFY 010	ARTIFICIAL INTELLIGENCE	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Explain the fundamental principles and techniques of Artificial Intelligence (AI).

COB2: Analyse the strengths and limitations of knowledge representation, problem-solving, and learning techniques in the context of engineering applications.

COB3: Design intelligent systems by applying AI techniques to solve defined computational problems.

COB4: Evaluate various AI methods based on their theoretical foundations and practical relevance.

COB5: Select and justify suitable AI techniques to address specific engineering problems

PREREQUISITES Probability, linear algebra and data structures

MODULE I ARTIFICIAL INTELLIGENCE AND ITS ISSUES **L:6 T:0 P:0**

Importance of AI, Evolution of AI - Applications of AI, Classification of AI systems, Knowledge Inferring systems and Planning, Uncertainty and Learning Systems.

MODULE II PROBLEM SOLVING TECHNIQUES **L:9 T:0 P:0**

Problem solving by Search, Problem space - State space, Blind Search - Types, Performance measurement.

MODULE III HEURISTIC SEARCH AND KNOWLEDGE BASED SYSTEMS **L:10 T:0 P:0**

Min-max algorithm, Alpha-Beta Pruning, Logical systems, Knowledge Based systems, Propositional Logic Constraints, Predicate Logic-First Order Logic, Ontological representations and applications.

MODULE IV UNCERTAINTY AND KNOWLEDGE REASONING **L:10 T:0 P:0**

Overview of uncertainty, Bayes Rule Inference, Belief Network, Utility Based System, Decision Network.

MODULE V LEARNING SYSTEMS AND EXPERT SYSTEMS **L:10 T:0 P:0**

Forms of Learning Types - Supervised, Unsupervised, Reinforcement Learning, Learning Decision Trees, Expert Systems - Stages in the development of an Expert System - Probability based Expert Systems - Expert System Tools - Difficulties in Developing Expert Systems – Applications of Expert Systems.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Russell, S. and Norvig, P, “Artificial Intelligence - A Modern Approach”, 3rd edition, Prentice Hall, 2016.
2. Poole, D. and Mackworth, A, “Artificial Intelligence: Foundations of Computational Agents, Cambridge University Press, 2017.

REFERENCES:

1. Rich, E., Knight, K and Shankar, B. “Artificial Intelligence”, 3rd edition, Tata McGraw Hill, 2019.
2. Luger, G.F.,” Artificial Intelligence -Structures and Strategies for Complex Problem Solving” 6th edition, Pearson, 2008.
3. Brachman, R. and Levesque, H., “Knowledge Representation and Reasoning”, Morgan Kaufmann, 2004.
4. Alpaydin, E, “Introduction to Machine Learning. 2nd edition, MIT Press, 2014
5. Sutton R.S. and Barto, A.G.,” Reinforcement Learning: An Introduction”, MIT Press, 2018.
6. Padhy, N.P., “Artificial Intelligence and Intelligent Systems”, Oxford University Press, 2009.

COURSE OUTCOMES:

COB1: Evaluate various Artificial Intelligence (AI) methods and explain their theoretical foundations.

COB2: Apply AI techniques for problem solving, inference, perception, knowledge representation, and learning.

COB3: Demonstrate the use of reasoning and knowledge representation in addressing real-world problems.

COB4: Analyze the role of search algorithms in AI-based problem solving.

COB5: Describe the components and development process of learning systems and expert systems.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2	-	1	-	3	2	-
CO2	3	3	3	2	2	1	3	3	2
CO3	2	3	2	2	2	-	2	3	2
CO4	3	2	3	3	2	-	2	2	1
CO5	2	2	2	2	3	1	2	3	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement:

This course will deliver the basic concepts of neural networks which is mostly used in Artificial Intelligence.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

Artificial intelligence plays major roles in industry and modern infrastructures. Innovative ideas can be implemented by programming.

ECFY 011	INDUSTRIAL IoT	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Understand IoT architecture and technology fundamentals in real-world systems.

COB2: Analyze communication technologies and classify common IoT communication protocols.

COB3: Evaluate hardware platforms and their corresponding networking configuration techniques.

COB4: Discuss frontend and backend development tools used in IoT.

COB5: Apply and create IoT solutions for relevant real-time applications.

PREREQUISITES:

Fundamentals of Computer Networks and Embedded Systems

MODULE I INTRODUCTION L:9 T: 0 P: 0

IoT- Architectural Overview – Design principles - IoT Technology Fundamentals Devices and gateways, Local and wide area networking, Data management, Business processes in IoT- Interoperability - Types of Interoperability Connectivity, Interoperability at Present state - Key Challenges- Introduction to Web Servers and Cloud Computing - Basics of Big Data and Data Science.

MODULE II IoT ARCHITECTURE AND APPLICATIONS L: 9 T: 0 P: 0

Architecture: M2M – Machine to Machine, Web of Things, IoT protocol, Introduction to wireless and mobile networks, ZigBee, BLE mesh, WiFi, LoRa, Applications: remote monitoring & sensing, remote controlling, performance analysis.

MODULE III IoT PLATFORM OVERVIEW L: 9 T: 0 P: 0

Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment – Router, Switches,

Overview and working principle of Wireless Networking equipment, Linux Network configuration Concepts.

MODULE IV IoT APPLICATION DEVELOPMENT L: 9 T: 0 P: 0

Application Protocols-MQTT, REST/HTTP, CoAP, MySQL -Back-end Application - Design Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android App Development tools.

MODULE V CASE STUDY & ADVANCED IoT APPLICATIONS L: 9 T: 0 P: 0

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Comparison of Industry 4.0 Factory and Today's Factory, Trends of Industrial Big Data and Predictive Analytics for Smart Business Transformation. Sensors and sensor Node and interfacing using any Embedded target boards.Security: Web security, conventional web technology and relationship with IIOT, Vulnerabilities of IoT, Privacy, Security requirements.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. Jean-Philippe Vasseur, Adam Dunkels, “Interconnecting Smart Objects with IP: The Next Internet”, Morgan Kuffmann-2010
2. Vijay Madisetti ,ArshdeepBahga, : Internet of Things (A Hands-on Approach) -2015
3. Adrian McEwen (Author), Hakim Cassimally, “Designing the Internet of Things” ,Wiley -2015
4. Dr. OvidiuVermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems,” River Publishers -2013.

REFERENCES:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Edition, Academic Press, 2014.
2. Barrie Sosinsky, “Cloud Computing Bible”, Wiley-India, 2010
3. Asoke K Talukder and Roopa R Yavagal, “Mobile Computing,” Tata McGraw Hill, 2017.
4. Adelstein and S.K.S. Gupta, “Fundamentals of Mobile and Pervasive Computing”, McGraw Hill, 2009.
5. Ronald L. Krutz, Russell Dean Vines, “Cloud Security: A Comprehensive Guide to Secure Cloud Computing”, Wiley-India, 2011

Giacomo Veneri, and Antonio Capasso, Hands-on Industrial Internet of Things: Create a powerful industrial IoT infrastructure using Industry 4.0, 2018, Packt Publishing.

COURSE OUTCOMES: After successful completion of the course, the student will be able to:

CO1: Understand IoT fundamentals, architecture, cloud computing, and core devices.

CO2: Analyze protocols and apply architecture concepts to IoT applications.

CO3: Configure networks and apply hardware platforms for IoT systems.

CO4: Evaluate and implement IoT applications using development and communication tools.

CO5: Create IoT projects and recommend technologies for advanced applications.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	3	2	2	3	3	1
CO2	3	2	3	3	3	2	3	3	2

CO3	3	1	3	3	3	2	3	3	1
CO4	2	3	3	3	3	3	3	3	3
CO5	3	3	3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement: The architecture and applications of IoT are explored in real time systems

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement : Industry standard protocols and platforms of IoT are studied

ECFY 012	MACHINE LEARNING AND DEEP	L	T	P	C
SDG: 4,9	LEARNING FOR EMBEDDED SYSTEMS	3	0	0	3

COURSE OBJECTIVES:

COB1: To provide a strong foundation in regression and classification models.

COB2: To explore hardware and software platforms used in embedded machine learning systems.

COB3: To analyze and evaluate the performance of machine learning algorithms on embedded systems.

COB4: To introduce the core concepts and principles of quantum machine learning.

COB5: To apply machine learning techniques to real-world applications across various domains.

MODULE I SUPERVISED AND UNSUPERVISED LEARNING ALGORITHMS **L:9 T:0 P:0**

Introduction to Machine Learning(ML) techniques, Regression - Gradient Descent, Classification- Logistic Regression, Support vector machines, K Nearest Neighbours, Decision Tree. K-Means clustering Algorithm, Hierarchical clustering- Dimensionality Reduction techniques - Artificial neural network

MODULE II MACHINE LEARNING ON EMBEDDED DEVICES **L:9 T:0 P:0**

Machine Learning Specific Hardware and Software- Machine Learning on Microcontrollers- Getting Started with Edge Impulse- Data Collection- Feature Extraction from Motion Data- Feature Selection in Edge Impulse- Machine Learning Pipeline

MODULE III ML MODEL EVALUATION AND DEPLOYMENT **L: 9 T: 0 P:0**

Model Training in Edge Impulse- Underfitting and Overfitting- Use a Model for Inference- Testing Inference with a Smartphone- Deploying a Trained Model to embedded board -Anomaly Detection

MODULE IV QUANTUM MACHINE LEARNING L: 9 T: 0 P:0

Basics of Quantum Computing: Qubits, superposition, entanglement- Quantum gates (X, H, CNOT, etc.)- Quantum circuits- Measurement and collapse- Variational Quantum Circuits (VQCs)- Quantum Neural Networks (QNN)- Quantum PCA- Quantum k-Means and clustering

MODULE V CASE STUDY L:9 T:0 P:0

Motion Detection-image detection-video classfication-Deployment of Tiny ML in Edge devices with sensor fusion- Introduction to Qiskit / PennyLane / Cirq- Simulating quantum circuitsHands-building a quantum circuit.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOK:

1. Machine Learning in Production: From Models to Products, Christian Kästner, Carnegie Mellon Universit,MIT Press ,2025
2. Machine Learning Algorithms in Depth,VadimSmolyakov,Manning, 2024
3. Ethemlpaydin, ”Introduction to Machine Learning”, MIT Press, Prentice Hall of India, Third Edition, 2014.

REFERENCES:

1. Ian H. Witten, Eibe Frank, Mark A. Hall, “Data Mining: Practical Machine Learning Tools and Techniques”, 3rd Edition, Morgan Kaufmann, 2011.
2. Thinking machines- SHIGEYUKI0 , Academic Press, 2021.
3. Quantum Computation and Quantum Information- Michael A. Nielsen & Isaac L. Chuang, CAMBRIDGE UNIVERSITY PRESS 2010
4. Quantum Machine Learning, Peter Wittek (Author), Academic Press,2014

COURSE OUTCOMES:

COB1: Select and apply appropriate mathematical techniques to solve machine learning problems.

COB2: Design and implement machine learning models on modern embedded system platforms.

COB3: Apply optimization techniques to enhance the performance of embedded machine learning systems.

COB4: Understand and explain the foundational concepts of quantum machine learning.

COB5: Utilize machine learning methods to solve real-world problems across various application domains

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2	2	2	-	2	2	2
CO2	3	2	2	2	2	-	2	2	2
CO3	3	2	3	2	2	-	2	2	2
CO4	3	2	3	2	3	-	2	2	2
CO5	3	2	3	2	3	3	2	2	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong opportunities for all.

Statement:

This course will deliver the basic concepts of neural networks which is mostly used in Artificial Intelligence machine systems

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

This course will deliver the concepts to design and innovate different types of embedded systems which will enhance quality of life and to meet industry requirements.

ECFY 013	REAL TIME SYSTEMS	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To understand the fundamental concepts of real-time systems and performance metrics.

COB2: To explore real-time programming languages and development tools with a focus on multitasking and timing specifications.

COB3: To analyze the unique features and challenges of real-time databases and ensure predictability.

COB4: To study real-time communication protocols, media, and fault-tolerant communication techniques.

COB5: To learn fault-tolerant strategies and reliability evaluation in real-time systems.

MODULE I INTRODUCTION TO REAL TIME SYSTEM **L:9 T:0 P:0**

Introduction –characterizing real time system -Performance Measures for Real Time Systems – Estimating Program Run Times – Task Assignment and Scheduling.

MODULE II PROGRAMMING LANGUAGES AND TOOLS **L:9 T:0 P:0**

Desired language characteristics – ADA language - Data typing – Control structures – Facilitating Hierarchical Decomposition- Packages- Run time Error handling – Overloading and Generics – Multitasking – Timing Specifications – Programming Environments – Run time support.

MODULE III REAL TIME DATABASES **L:9 T:0 P:0**

Basic Definition, Real time Vs General Purpose Databases- Main Memory Databases- Transaction priorities-Transaction Aborts-Concurrency control issues-Disk Scheduling Algorithms-Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

MODULE IV REAL TIME COMMUNICATION L:9 T:0 P:0

Communications media, Network Topologies, Protocols- contention based, Token based, Stop-and-Go multihop, Polled Bus, Hierarchical Round Robin Protocol, Deadline-Based Protocols, Fault Tolerant Routing.

MODULE V FAULT TOLERANT AND EVALUATION TECHNIQUES L:9 T:0 P:0

Fault Tolerance Techniques – Fault Types – Fault Detection-Fault and Error containment- Redundancy- Reliability Evaluation Techniques – Software error models.

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 2010
2. Rajib Mall, ”Real-time systems: theory and practice”, Pearson Education, 2007.
3. Peter D.Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.

REFERENCES:

1. Xiaocong Fan, “Real-Time Embedded Systems: Design Principles and Engineering Practices”, Elsevier, 2015.
2. Albert M. K. Cheng, “Real-Time Systems: Scheduling, Analysis, and Verification“,Wiley publishers, 2003.
3. P. A. Laplante," Real-Time Systems Design & Analysis", Willey, 2011.
4. Qing Li, "Real Time Concepts for Embedded Systems", Elsevier, 2011.

COURSE OUTCOMES:

COB1: Characterize real-time systems, evaluate performance, and apply scheduling techniques effectively.

COB2: Develop and analyze real-time programs using ADA and other tools, considering hierarchical structures and multitasking.

COB3: Differentiate real-time databases from general databases and apply concurrency and transaction control.

COB4: Evaluate real-time communication protocols and topologies for fault-tolerant data exchange.

COB5: Analyze and apply fault detection, containment, and reliability models in real-time systems.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2		1		3	2	3
CO2	3	3	3	2	2	1	3	3	3
CO3	2	3	2	2	2		2	3	2
CO4	3	2	3	3	2		2	2	3
CO5	2	2	2	2	3	1	2	3	2

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

The various industrial standards of technical drawing and the application of orthographic projections to draw simple solids helps to innovate a new design for sustainable industrialization

ECFY 014	MULTICORE ARCHITECTURE	L	T	P	C
SDG: 4, 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To explore advanced principles in the design and quantitative analysis of modern processor and multicore architectures.

COB2: To investigate data-level parallelism in vector and SIMD architectures, including their implementation in GPUs.

COB3: To examine thread-level parallelism and associated challenges in shared and distributed memory multiprocessors.

COB4: To analyze large-scale system architectures and their relevance in warehouse-scale and cloud computing environments.

COB5: To develop an understanding of GPU programming models and optimization techniques using CUDA and OpenCL.

MODULE I ADVANCED FUNDAMENTALS OF MULTICORE ARCHITECTURE DESIGN **L:9 T: 0 P: 0**

Classes of Computers and Design Principles - Trends in Power, Energy, and Technology Scaling - Quantitative Analysis: Performance, Cost, and Energy Trade-offs - Dependability and Fault Tolerance Basics - Classes of Parallelism: ILP, DLP, TLP, RLP - Pipeline Design and Hazards (Structural, Data, Control) - Superscalar, VLIW, and Out-of-Order Execution - Introduction to NoC (Network-on-Chip) as Single-core Bottleneck Solution - Single-Core Limitations and the Need for Multicore

MODULE II DATA LEVEL PARALLELISM AND VECTOR COMPUTATION **L: 9 T: 0 P: 0**

Vector Processor Architecture and Applications - SIMD Architectures in Multimedia and DSP - SIMD Instruction Set Extensions: Intel SSE/AVX, ARM NEON - GPU-Based SIMD: Execution Model and Warp Scheduling - Loop Unrolling and Software Vectorization - Automatic Vectorization in Compilers - Introduction to OpenCL Programming Model

MODULE III THREAD LEVEL PARALLELISM AND MULTIPROCESSORS **L: 9 T: 0 P: 0**

Shared vs Distributed Memory Models - Symmetric Multiprocessing (SMP) and Cache Coherence - Coherence Protocols: MESI, MOESI, Directory-Based Approaches - Memory Consistency Models: SC, TSO, Release Consistency - Synchronization Mechanisms: Locks, Barriers, Atomic Operations - Introduction to OpenMP and PThreads - Performance and Scalability Analysis - Interconnect Architectures: Buses, Crossbar, Mesh, Multistage Networks

MODULE IV RLP, SCALABILITY, AND WAREHOUSE-SCALE ARCHITECTURES **L: 9 T: 0 P: 0**

Workloads and Programming Models for Warehouse-Scale Systems - Cluster and Data Center Architecture: Google Warehouse-Scale Design - Virtualization and Containerization in Multicore Systems (VMs vsDocker) - Power and Cooling Considerations in Datacenters - Fault Tolerance and Reliability at Scale - Energy-Proportional Computing - Cloud Resource Allocation and Scheduling

MODULE V GPU ARCHITECTURE AND PARALLEL PROGRAMMING **L: 9 T: 0 P: 0**

GPU Architecture Evolution: NVIDIA, AMD, Apple GPU - Typical Streaming Multiprocessor Design - CUDA Programming Model: Threads, Blocks, Grids, Warps - Scheduling Strategies: SIMT Execution and Warp Divergence - Memory Hierarchy: Shared, Global, Constant, Texture Memory - Optimization Strategies: Coalescing, Bank Conflicts, Occupancy - Comparison of CUDA vsOpenCLvsVulkan Compute - Profiling and Debugging using Nsight / Visual Profiler

L – 45; T – 0; P – 0; Total Hours:45

TEXT BOOKS:

1. David B. Kirk, Wen-mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, 4th Edition, Morgan Kaufmann, 2022.

2. Hyesoon Kim, GPU Computing Gems: Emerald Edition, Elsevier/Morgan Kaufmann, 2021.
3. Vivek S. Seshadri, Computer Architecture: A Systems Design Approach, Morgan Kaufmann, 2020.

REFERENCES:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 6th Edition, Morgan Kaufmann, 2019 (latest edition available).
2. Robert Robey, Yuliana Zamora, Parallel and High Performance Computing, Manning Publications, 2021.
3. Benedict R. Gaster et al., Heterogeneous Computing with OpenCL 2.0, Morgan Kaufmann, 2020.

COURSE OUTCOMES:

CO1: Analyze the performance and scalability aspects of processor architectures using quantitative methods.

CO2: Illustrate data-level parallelism through vector, SIMD, and multimedia processing techniques.

CO3: Evaluate thread-level parallelism, coherence protocols, and synchronization in multiprocessor systems.

CO4: Assess the design, infrastructure, and energy considerations of warehouse-scale and cloud architectures.

CO5: Implement and optimize parallel applications using GPU programming models such as CUDA and OpenCL.

Board of Studies (BoS):

27th BOS of Department of ECE held on 26.06.2025

Academic Council:

24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2		3	2		1	3	2	
CO2			3	3		1	3	3	
CO3	2		3	3	2	1	3	3	2
CO4	1	2	3		3	3	2	2	2
CO5	2	2	3	3	3	3	3	3	3

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement:

The course equips students with essential knowledge in parallel computing, promoting lifelong learning in advanced computing technologies.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

Multicore architectural knowledge directly contributes to innovation in scalable and energy-efficient computing systems used in industrial and embedded domains.

ECFY 015	MODERN ANTENNA THEORY AND	L	T	P	C
SDG:9	APPLICATIONS	3	0	0	3

COURSE OBJECTIVES:

COB1: Understand antenna fundamentals in millimeter-wave and beyond.

COB2: Design compact antennas suitable for mmWave with enhanced bandwidth and efficiency.

COB3: Develop array antennas with beamforming and beam steering techniques.

COB4: Analyze MIMO antenna systems and metasurface-assisted beam steering for enhanced performance.

COB5: Acquire skills in antenna measurements, simulations, and apply knowledge to advanced wireless systems like 5G, 6G, and IoT.

MODULE I ANTENNA FUNDAMENTALS FOR MMWAVE AND 6G **L:6 T:2 P:0**

Electromagnetic spectrum for mmWave (30–300 GHz) and terahertz ,Fundamental antenna parameters and their variation at mmWave, Physical limitations: skin depth, conductor/dielectric losses at mmWave,Challenges in mmWave antenna design: miniaturization, fabrication tolerances, Basics of simulation tools for mmWave (CST, HFSS, ADS).

MODULE II ADVANCED ANTENNA STRUCTURES AND FEEDING TECHNIQUES **L:6 T: 2 P:0**

Planar antennas: Microstrip patch, slot, Vivaldi antennas, Feeding techniques at mmWave: Coplanar Waveguide (CPW), Substrate Integrated Waveguide (SIW), proximity coupling Bandwidth enhancement: Defected Ground Structure (DGS), slots, stacked configurations, Compact and conformal antenna designs for wearable and IoT mm Wave applications.

MODULE III ANTENNA ARRAYS AND BEAMFORMING FOR MMWAVE **L: 6 T: 2 P:0**

Array fundamentals: Linear, planar, and conformal arrays, Array factor, pattern multiplication, beam steering principles, Beamforming types: Analog, digital, and hybrid beam forming, Beam squinting, grating lobes, and mutual coupling at mm Wave, Massive MIMO arrays: Design constraints for 5G/6G base stations.

MODULE IV MIMO ANTENNAS AND METASURFACES WITH BEAM STEERING **L: 6 T:2 P:0**

MIMO antenna principles: Spatial diversity, multiplexing gain, channel capacity, mm Wave MIMO design: Isolation, compactness, polarization diversity Techniques for mutual coupling reduction: EBG, DGS, parasitic elements.

METASURFACES FOR BEAM STEERING:

Reconfigurable Intelligent Surfaces (RIS), Phase-gradient metasurfaces for dynamic beam steering,Beam steering without mechanical movement – electronically tunable metasurfaces, Applications in 5G, 6G, satellite, and IoT mm Wave networks.

MODULE V ANTENNA MEASUREMENTS AND EMERGING TECHNOLOGIES **L: 6 T: 2 P:0**

Antenna measurement facilities: Anechoic chamber, compact ranges, Measurement techniques: VSWR, return loss, gain, radiation pattern, axial ratio, Measurement challenges at mmWave frequencies, Emerging antenna technologies: Flexible, wearable, graphene-based, and THz antennas, Sustainable antenna design: Eco-friendly materials, energy-efficient structures.

L – 45; TOTAL HOURS:45

TEXT BOOKS:

1. Constantine A. Balanis, *"Antenna Theory: Analysis and Design"*, 5th Edition, Wiley, 2022.
2. Zhi Ning Chen and Kwai Man Luk, *"Antennas for 5G and Beyond"*, Wiley-IEEE Press, 2020.

REFERENCES:

1. Raghavan, S., *"mmWave Massive MIMO: A Paradigm for 5G and Beyond"*, Springer, 2020.

2. Hao Yang et al., *"Reconfigurable Intelligent Surface Empowered Wireless Communications"*, IEEE Communications Surveys & Tutorials, 2021.
3. Recent papers from *IEEE Transactions on Antennas and Propagation*, *IEEE Access*, and *Nature Communications*.

COURSE OUTCOMES:

COB1: Apply antenna fundamentals specific to mmWave communication.

COB2: Design wire, slot, and planar antennas addressing mmWave challenges.

COB3: Analyze and implement beamforming and beam steering using arrays at mmWave.

COB4: Design MIMO antenna systems and metasurface-based beam-steering solutions.

COB5: Apply measurement techniques to validate antenna designs for modern wireless systems.

Board of Studies (BoS): 27th BOS of Department of ECE held on 26.06.2025

Academic Council: 24th AC held on 26.08.2025

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	1	–-	3	–-	–-	1	1	1	–
CO2	1	–	3	–-	–-	3	1	1	–
CO3	3	1	3	–-	–-	1	1	1	-
CO4	3	1	3	–-	–-	3	1	1	3
CO5	1	3	3	–-	–-	1	1	1	1

Legend: L – Low (1), M – Medium (2), H – High (3).

SDG 9 – Industry, Innovation, and Infrastructure: The course contributes to sustainable industrialization and technological innovation by preparing students to design and develop advanced antenna systems for 5G, 6G, and IoT, enabling more efficient and sustainable wireless networks.

ECFY 016	NANOELECTRONICS AND	L	T	P	C
SDG:9	TECHNOLOGY	3	0	0	

COURSEOBJECTIVES:

COB1: To categorize nano-materials and the depositionTechniques.

COB2: To classify characterization of nano-materials.

COB3: To explain band structure models.

COB4: To select materials used for nano-electronics.

COB5: To show various electron transport mechanisms in nano structures.

PREREQUISITES: Fabrication in VLSI design, Atom and its Structures

MODULE I INTRODUCTION AND FABRICATION OF NANOMATERIALS 9

Overview of nanotechnology, Historical background, Importance of Nanoscale, Bottom-up approaches, Top-down approaches, Functional approaches - Difference between bulk and nano materials - Size dependent properties – Fundamentals of film-Physical vapor deposition(PVD)-Chemical Vapor deposition (CVD)-Atomic layer deposition-sol gel films

MODULE II SYNTHESIS AND CHARACTERIZATION OF NANOMATERIALS 9

Lithography-Assembly of nano-particles and nano-wires-other methods for micro fabrication - Structural characterization –X-ray diffraction, Small angle X-ray scattering, Scanning electron microscopy, Transmission electron microscopy, Scanning probe microscopy- Chemical characterization – Optical spectroscopy, Electron spectroscopy, Ion spectroscopy-Physical properties of nano-materials.

MODULE III FREE ELECTRON THEORY & THE NEW OHM'S LAW 9

Electron flow, Classical free electron theory, Sommerfeld's theory, The quantum of conductance, Coulomb blockade, Towards Ohm's law. The Elastic Resistor: Conductance of an Elastic Resistor, Elastic Resistor- Heat dissipation.

MODULE IV MATERIALS FOR NANO ELECTRONICS 9

Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor hetero structures, Lattice-matched and pseudo morphic hetero structures, Inorganic nano-wires, Organic semiconductors, Carbon nano materials: nano-tubes and fullerenes.

MODULE V ELECTRON TRANSPORT IN SEMICONDUCTORS AND NANO STRUCTURES 9

Time and length scales of the electrons in solids, Statistics of the electrons in solids and nano structures, Fermistatistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures.

L–45; TOTALHOURS –45

TEXTBOOKS:

1. Guozhong Cao, Ying Wang, “Nanostructures and Nano materials” world scientific series in nanoscience and nanotechnology 2nd edition 2016
2. Guozhong Cao,“Nanostructures and NanoMaterials-Synthesis, Properties and Applications”, Imperial College Press, 2011.
3. M.S. Ramachandra Rao, Shubra Singh H, “Nanoscience a nd Nanotechnology: Fundamentals to Frontiers”, Wiley, 2013.
4. Charles P. Poole, Jr., Frank J. Owens, Introduction to Nanotechnology, John Wiley & Sons, Inc, 2003.

REFERENCES:

1. C.Dupas, P.Houdy, M.Lahmani, “Nanoscience: Nano technologies and Nanophysics”, Springer-Verlag Berlin Heidelberg, 2007.
2. Mick Wilson, Kamali Kannangara, Michells Simmons and Burkhard Raguse,“NanoTechnology– Basic Science and Emerging Technologies”, 1st Edition, Overseas Press, New Delhi, 2005

COURSEOUTCOMES:

The students should be able to

CO1: infer the approaches used for fabricating the nano-materials.

CO2: apply the concept in synthesizing and characterizing nano material.

CO3: define the electron theory and ohm's law.

CO4: analyze the types of materials and the bonding.

CO5: compare the scaling of transistors and devices to smaller structures.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	M	-	M	M	-	-	M	-	-
CO2	M	H	H	-	M	-	H	H	M
CO3	M	M	H	H	M	-	H	H	H
CO4	H	M	H	H	H	-	M	H	H
CO5	M	H	H	-	H	M	H	H	-

Note:L-LowCorrelation M-MediumCorrelation H-High Correlation

SDG9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement:

The study on nano material, its deposition techniques helps in deep understanding of the nano electronics.

ECFY 017	ADVANCED BIOMEDICAL SIGNAL	L	T	P	C
SDG:9	PROCESSING	3	0	0	3

COURSEOBJECTIVES:

COB1: Understand the basics of human physiological signals.

COB2: Explain the characteristics and morphology of bio-signals.

COB3: Apply mathematical models to represent bio-signals.

COB4: Develop algorithms for event detection and feature extraction.

COB5: Analyze and reduce noise in biomedical signals.

PREREQUISITES: Digital Signal Processing

MODULE I INTRODUCTION - BIOMEDICAL SIGNAL PROCESSING 8

Basics of Bioelectrical Signals, Signal Acquisition and Analysis, Performance Evaluation. The Electrocardiogram – Electrical Activity of the Heart- A Brief Background, Heart Rhythms, Heartbeat Morphologies, Noise and Artifacts, Clinical Application.

MODULE II ECG SIGNAL PROCESSING AND HEART RATE VARIABILITY 12

Baseline Wander, Powerline Interference (50/60 Hz), Muscle Noise Filtering, QRS Detection, Wave Delineation, Data Compression.

Acquisition and RR Interval Conditioning, Time Domain Measures, Heart Rhythm Representations, Spectral Analysis of Heart Rate Variability, Clustering of Beat Morphologies.

MODULE III THE ELECTROENCEPHALOGRAM 12

Electrical Activity –a brief description, EEG Signal Processing, Modeling the EEG Signal, Artifacts in the EEG, Nonparametric Spectral Analysis.

Model-based Spectral Analysis, EEG Segmentation, Joint Time-Frequency Analysis, Evoked Potentials- Evoked Potential Modalities.

MODULE IV NOISE ELIMINATION TECHNIQUES 7

Noise Characteristics, Noise Reduction by Ensemble Averaging, Noise Reduction by Linear Filtering, Single-Trial Analysis Using Basic Functions, Adaptive Analysis using basis functions, Wavelets.

MODULE V THE ELECTROMYOGRAM 6

The Electrical Activity of Muscles, Amplitude Estimation in the Surface EMG, Spectral Analysis of the Surface EMG, Conduction Velocity Estimation, Modeling the intramuscular EMG, Intramuscular EMG Signal Decomposition

..

L–45; TOTALHOURS –45

TEXTBOOKS:

1. Sörnmo, “Bioelectrical Signal Processing in Cardiac & Neurological Applications”, Elsevier ,2005.
2. Rangaraj M Rangayyan, “Biomedical Signal Analysis”, Wiley 2002.

REFERENCES:

1. D.C.Reddy, “Biomedical Signal Processing: Principles and techniques” , Tata McGraw Hill, New Delhi, 2005
2. Willis J Tompkins, Biomedical Digital Signal Processing, Prentice Hall, 1993
3. Bruce, “Biomedical Signal Processing & Signal Modeling,” Wiley, 2001
4. Semmlow, “Biosignal and Biomedical Image Processing”, Marcel Dekker, 2004

COURSEOUTCOMES:

The students should be able to

CO1: Describe different physiological signals and their features.

CO2: Analyze bio-signal morphology and characteristics.

CO3: Model physiological signals mathematically.

CO4: Implement event detection algorithms.

CO5: Apply noise reduction and signal estimation techniques.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	H	M	L	L	L	-	M	L	-
CO2	H	H	M	M	M	-	H	M	-
CO3	H	H	M	H	H	-	H	H	M
CO4	H	H	H	H	H	-	H	H	M
CO5	H	H	M	H	H	-	H	H	M

Note:L-LowCorrelation M-MediumCorrelation H-High Correlation

SDG 9 – Industry, Innovation and Infrastructure

Statement:

Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation.