



**TIMING:**  
**FN-10.00AM – 12.00NOON &  
 AN-02.00PM - 04.00PM**

**CONVENOR**  
**Dr.D. NAJUMNISSA JAMAL**  
**DEAN(SECS)**  
**Dr. C. THARINI,**  
**Professor & Head/ECE**

**COORDINATORS**  
**Dr.V.Jeanshilpa,AP/ECE**  
**MS.S.Anusooya,AP/ECE**  
**MS.R.Anitha,AP(SG)/ECE**  
**Contact:9841721102**  
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**jeanshilpa@crescent.education**

**TRAINING FEE RS.250/-**  
**THROUGH GPAY @9841721102**

**Who can attend :**  
**UG & PG students,**  
**Faculty,Research scholars**  
**and Industry People**  
**Last date for Registration:**  
**27.04.2021**



B.S. Abdur Rahman  
**Crescent**  
 Institute of Science & Technology  
 Deemed to be University u/s 3 of the UGC Act, 1956

**Department of Electronics and Communication Engineering**  
**&**  
**Entuple Technologies ,Bangalore**  
**Jointly Organizes**

**“ONLINE TRAINING ON**  
**FULL CUSTOM AND SEMI CUSTOM DESIGN FLOW IN VLSI**  
**USING CADENCE TOOLS”**  
**ON 29.04.2021 & 30.04.2021**

DAY-1: SEMI CUSTOM DESIGN FLOW	DAY-2: FULL CUSTOM DESIGN FLOW
<ul style="list-style-type: none"> <li>➤ Cadence Design Flow</li> <li>➤ Overview of features &amp; new tools</li> <li>➤ Functional Verification flow using Incisive</li> <li>➤ RTL Synthesis &amp; DFT flow using Genus</li> <li>➤ PD flow with Innovus</li> <li>➤ STA with Tempus</li> <li>➤ Static &amp; Dynamic Power Analysis with Voltus</li> <li>➤ Logical Equivalence Check with Conformal</li> </ul>	<ul style="list-style-type: none"> <li>➤ Schematic Capture using Virtuoso Schematic Editor</li> <li>➤ Functional Simulation using Spectre</li> <li>➤ Schematic driven Layout Design using Virtuoso Layout Editor</li> <li>➤ Physical Verification which includes DRC &amp; LVS using Assura</li> <li>➤ Parasitic Extraction</li> <li>➤ Post Layout Simulation</li> <li>➤ Generation of GDSII</li> </ul>

Session will be handled by Industrial experts from Entuple Technologies

**Registration Link:**  
**<https://forms.gle/Bv7kWbrghjQn2PU1A>**

