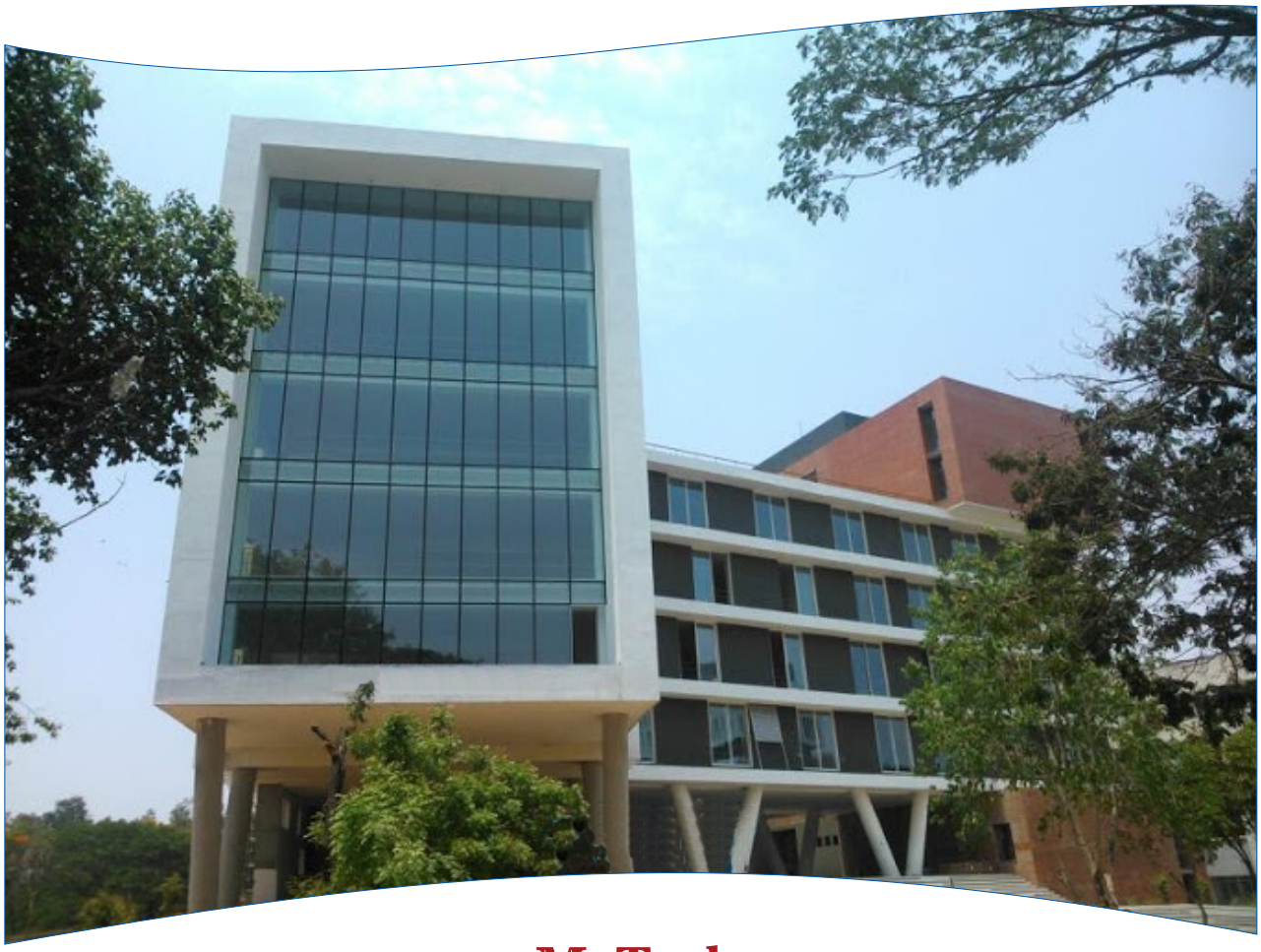
CURRICULUM AND SYLLABI

REGULATIONS - 2016

(As approved by the 9th Academic Council)



M. Tech.

VLSI and EMBEDDED SYSTEMS

B.S.ABDUR RAHMAN UNIVERSITY

B.S. ABDUR RAHMAN INSTITUTE OF SCIENCE & TECHNOLOGY
(Estd. u/s 3 of the UGC Act, 1956)

(FORMERLY B.S. ABDUR RAHMAN CRESCENT ENGINEERING COLLEGE)
Rated with A Grade by National Assessment and Accreditation Council
Seethakathi Estate, G.S.T. Road, Vandalur, Chennai - 600 048
www.bsauniv.ac.in

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JULY 2016

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UNIVERSITY VISION AND MISSION

VISION

B.S. Abdur Rahman Institute of Science and Technology aspires to be a leader in Education, Training and Research in Engineering, Science, Technology and Management and to play a vital role in the Socio-Economic progress of the Country.

MISSION

- To blossom into an internationally renowned University
- To empower the youth through quality education and to provide professional leadership
- To achieve excellence in all its endeavors to face global challenges
- To provide excellent teaching and research ambience
- To network with global institutions of Excellence, Business, Industry and Research Organizations
- To contribute to the knowledge base through Scientific enquiry, Applied research and Innovation

VISION AND MISSION OF THE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Department of Electronics and Communication Engineering envisions to be a leader in providing state of the art education through excellence in teaching, training, and research in contemporary areas of Electronics and Communication Engineering and aspires to meet the global and socio economic challenges of the country.

MISSION

- The Department of Electronics and Communication Engineering endeavors to produce globally competent Engineers prepared to face challenges of the society.
- To enable the students to formulate, design and solve problems in applied science and engineering.
- To provide excellent teaching and research environment using state of the art facilities.
- To provide adequate practical training to meet the requirement of the Electronics & communication industry.
- To train the students to take up leadership roles in their career or to pursue higher education and research.

PROGRAMME EDUCATIONAL OBJECTIVES AND OUTCOMES

PROGRAMME EDUCATIONAL OBJECTIVES:

The objective of the program is

PEO 1 To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design

PEO 2 To provide technical skills in software and hardware tools related to the design and implementation of integrated Circuits, System on Chip for real time applications

PEO 3 To provide scope for Applied Research and innovation in the various fields of VLSI and Embedded Systems, and enabling the students to work in the emerging areas

PEO 4 To enhance communication and soft skills of students to make them work effectively as a team

PROGRAM OUTCOMES:

The graduates will

PO1 Be able to analyze, design and implement Analog, Digital and Mixed Signal Circuits and real time embedded systems

PO2 Have in-depth knowledge and capability to use industry standard tools in the design and implementation of VLSI and real time Embedded Systems.

PO3 Be able to undertake research projects in related domains of VLSI and Embedded systems.

PO4 Possess the capability to communicate effectively and work as a team in the professional career

REGULATIONS – 2016
FOR
M. Tech. / MCA / M.Sc. DEGREE PROGRAMMES

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires

i. **"Programme"** means a Post Graduate Degree Programme (M. Tech. / MCA / M.Sc.)

ii. **"Course"** means a theory or practical subject that is normally studied in a semester, like Applied Mathematics, Structural Dynamics, Computer Aided Design, etc.

iii. **"University"** means B.S. Abdur Rahman University, Chennai, 600048.

iv. **"Institution"** unless otherwise specifically mentioned as an autonomous or off campus institution means B.S. Abdur Rahman University.

v. **"Academic Council"** means the Academic Council, which is the apex body on all academic matters of this University

vi. **"Dean (Academic Affairs)"** means Dean (Academic Affairs) of B.S. Abdur Rahman University, who administers the academic matters.

vii. **"Dean (P.G. Studies)"** means Dean (P.G. Studies) of B.S. Abdur Rahman University who administers all P.G Programmes of the University in coordination with Dean (Academic Affairs)

viii. **"Dean (Student Affairs)"** means Dean (Student Affairs) of B.S. Abdur Rahman University, who looks after the welfare and discipline of the students.

ix. **"Controller of Examinations"** means the Controller of Examinations of B.S. Abdur Rahman University who is responsible for conduct of examinations and declaration of results.

2.0 PROGRAMMES OFFERED, MODE OF STUDY AND ADMISSION REQUIREMENTS

2.1 P.G. Programmes Offered

The various P.G. Programmes and their modes of study are as follows:

Degree	Mode of Study
M. Tech. /M.C.A. / M.Sc.	Full Time & Part Time – Day / Evening / Weekends

2.2 Modes of Study

2.2.1 Full-time

Students admitted under "Full-Time" shall be available in the Institution during the complete working hours for curricular, co-curricular and extra-curricular activities assigned to them.

2.2.2 A full time student, who has completed all non-project courses desiring to do the Project work in part-time mode for valid reasons, shall apply to the Dean (Academic Affairs) through the Head of the Department. Permission may be granted based on merits of the case. Such conversion is not permitted in the middle of a semester.

2.2.3 Part-time

In this mode of study, the students are required to attend classes for the courses in the time slots selected by them, during the daytime (or) evenings (or) weekends.

2.3 Admission Requirements

2.3.1 Students for admission to the first semester of the Master's Degree Programme shall be required to have passed the appropriate degree examination of this University as specified in the Table shown for eligible entry qualifications for admission to P.G. programmes or any other degree examination of any University or authority accepted by this University as equivalent thereto.

2.3.2 Eligibility conditions for admission such as class obtained, number of attempts in the qualifying examination and physical fitness will be as prescribed by this Institution from time to time.

2.3.3 All part-time students should satisfy other conditions regarding experience, sponsorship etc., which may be prescribed by this Institution from time to time.

2.3.4 Student eligible for admission to M.C.A under lateral entry scheme shall be required to have passed three year degree in B.Sc (Computer Science) / B.C.A / B.Sc (Information Technology)

3.0 DURATION AND STRUCTURE OF THE P.G. PROGRAMME

3.1 The minimum and maximum period for completion of the P.G. Programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M. Tech. (Full Time)	4	8
M. Tech. (Part Time)	6	12
M.C.A. (Full Time)	6	12
M.C.A. (Part Time)	9	18
M.C.A. (Full Time) – (Lateral Entry)	4	8
M.C.A. (Part Time) – (Lateral Entry)	6	12
M.Sc. (Full Time)	4	8
M. Sc. (Part Time)	6	12

3.2 The PG. programmes consist of the following components as prescribed in the respective curriculum

i. Core courses
ii. General Elective courses
iii. Professional Elective courses
iv. Project work / thesis / dissertation
v. Laboratory Courses
vi. Case studies
vii. Seminars
viii. Mini Project
ix. Industrial Internship

3.3 The curriculum and syllabi of all PG. programmes shall be approved by the Academic Council of this University.

3.4 The minimum number of credits to be earned for the successful completion of the programme shall be specified in the curriculum of the respective specialization of the P.G. programme.

3.5 Each academic semester shall normally comprise of 80 working days. Semester-end examinations will follow immediately after the last working day.

ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO P.G. PROGRAMMES

Sl. No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
01	Civil Engineering	M. Tech. (Structural Engineering)	B.E / B. Tech. (Civil Engineering) / (Structural Engineering)
		M. Tech. (Construction Engineering and Project Management)	
02	Mechanical Engineering	M. Tech. (Manufacturing Engineering)	B.E. / B. Tech. (Mechanical / Auto / Manufacturing / Production / Industrial / Mechatronics / Metallurgy / Aerospace /Aeronautical / Material Science / Marine Engineering)
		M. Tech. (CAD/CAM)	
03	Polymer Engineering	M. Tech. (Polymer Technology)	B. E. / B. Tech. Mechanical / Production /Polymer Science or Engg or Tech / Rubber Tech / M.Sc (Polymer Sc./ Chemistry Appl. Chemistry)
04	Electrical and Electronics Engineering	M. Tech. (Power Systems Engg)	B.E / B.Tech (EEE / ECE / E&I / I&C / Electronics / Instrumentation)
		M. Tech. (Power Electronics & Drives)	B.E / B.Tech (EEE / ECE / E&I / I&C / Electronics / Instrumentation)
05	Electronics and Communication Engineering	M. Tech. (Communication Systems)	B.E / B.Tech (EEE/ ECE / E&I / I&C / Electronics / Instrumentation)
		M. Tech. (VLSI and Embedded Systems)	B.E. / B. Tech. (ECE / Electronics / E&I / I&C / EEE)
06	ECE Department jointly with Physics Dept.	M. Tech. (Optoelectronics and Laser Technology)	B.E. / B. Tech. (ECE / EEE / Electronics / EIE / ICE) M.Sc (Physics / Materials Science / Electronics / Photonics)
07	Electronics and Instrumentation Engineering	M. Tech. (Electronics and Instrumentation Engineering)	B.E. / B. Tech. (EIE / ICE / Electronics / ECE / EEE)

Sl. No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
08	Computer Science and Engineering	M. Tech. (Computer Science and Engineering)	B.E. / B. Tech. (CSE / IT / ECE / EEE / EIE / ICE / Electronics / MCA)
		M. Tech. (Software Engineering)	B.E. / B. Tech. (CSE / IT) MCA
		M. Tech. (Network Security)	B.E. / B. Tech. (CSE / IT / ECE / EEE / EIE / ICE / Electronics / MCA)
		M. Tech. (Computer Science and Engineering with specialization in Big Data Analytics)	B.E. / B. Tech. (CSE / IT / ECE / EEE / EIE / ICE / Electronics / MCA)
09	Information Technology	M. Tech. (Information Technology)	B.E / B. Tech. (IT / CSE / ECE / EEE / EIE / ICE / Electronics) MCA
		M. Tech. (Information Security & Digital Forensics)	B.E / B. Tech. (IT / CSE / ECE / EEE / EIE / ICE / Electronics) MCA
10	Computer Applications	M.C.A.	Bachelor Degree in any discipline with Mathematics as one of the subjects (or) Mathematics at +2 level
		M.C.A. – (Lateral Entry)	B.Sc Computer Science / B.Sc Information Technology / B.C.A
		M. Tech. (Systems Engineering and Operations Research)	BE / B. Tech. (Any Branch) or M.Sc., (Maths / Physics / Statistics / CS / IT / SE) or M.C.A.
		M. Tech. (Data & Storage Management	BE / B. Tech. (Any Branch) or M.Sc., (Maths / Physics / Statistics / CS / IT / SE) or M.C.A.
11	Mathematics	M.Sc. (Actuarial Science)	Any Degree with Mathematics / Statistics as one of the subjects of study.
		M.Sc. Mathematics	B.Sc. (Mathematics)
12	Physics	M.Sc.(Physics)	B.Sc.(Physics / Applied Science / Electronics / Electronics Science / Electronics & Instrumentation)
		M.Sc. (Material Science)	B.Sc.(Physics / Applied Science / Electronics / Electronics

Sl. No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
			Science / Electronics & Instrumentation)
13	Chemistry	M.Sc.(Chemistry)	B.Sc (Chemistry / Applied Science)
14	Life Sciences	M.Sc. Molecular Biology & Biochemistry	B.Sc. in any branch of Life Sciences
		M.Sc. Genetics	B.Sc. in any branch of Life Sciences
		M.Sc. Biotechnology	B.Sc. in any branch of Life Sciences
		M.Sc. Microbiology	B.Sc. in any branch of Life Sciences
		M.Sc. Bioscience	B.Sc. in any branch of Life Sciences
		M. Tech. Biotechnology	B. Tech. (Biotechnology / Chemical Engineering) / M.Sc. in any branch of Life Sciences

3.6 The curriculum of PG programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below:

Programme	Minimum prescribed credits
M. Tech.	73
M.C.A.	120
M.Sc.	72

3.7 Credits will be assigned to the courses for all P.G. programmes as given below:

- One credit for one lecture period per week (or) 15 periods per semester
- One credit for one tutorial period per week
- One credit each for seminar/practical session/project of two or three periods per week
- One credit for two weeks of industrial internship
- One credit for 15 periods of lecture (can even be spread over a short span of time)

3.8 The number of credits registered by a student in non-project semester and project semester should be within the range specified below:

P.G. Programme	Full Time		Part Time	
	Non-project Semester	Project semester	Non-project Semester	Project semester
M. Tech.	9 to 28	12 to 28	6 to 12	12 to 28
M.C.A.	9 to 29	12 to 29	6 to 12	12 to 29
M.Sc.	9 to 25	12 to 20	6 to 12	12 to 20

3.9 The student may choose a course prescribed in the curriculum from any department depending on his / her convenient time slot. All attendance will be maintained course-wise only.

3.10 The electives from the curriculum are to be chosen with the approval of the Head of the Department.

3.11 A student may be permitted by the Head of the Department to choose electives from other PG programmes either within the Department or from other Departments up to a maximum of nine credits during the period of his/her study, with the approval of the Head of the Departments offering such courses.

3.12 To help the students to take up special research areas in their project work and to enable the department to introduce courses in latest/emerging areas in the curriculum, "Special Electives" may be offered. A student may be permitted to register for a "Special Elective" up to a maximum of three credits during the period of his/her study, provided the syllabus of this course is recommended by the Head of the Department and approved by the Chairman, Academic Council before the commencement of the semester, in which the special elective course is offered. Subsequently, such course shall be ratified by the Board of Studies and Academic Council.

3.13 The medium of instruction, examination, seminar and project/thesis/ dissertation reports will be English.

3.14 Industrial internship, if specified in the curriculum shall be of not less than two weeks duration and shall be organized by the Head of the Department.

3.15 Project Work / Thesis / Dissertation

3.15.1 Project work / Thesis / Dissertation shall be carried out under the supervision of a Faculty member in the concerned Department.

3.15.2 A student may however, in certain cases, be permitted to work for the project in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from

the organization and the student shall be instructed to meet the faculty periodically and to attend the review committee meetings for evaluating the progress.

3.15.3 Project work / Thesis / Dissertation (Phase - II in the case of M. Tech.) shall be pursued for a minimum of 16 weeks during the final semester, following the preliminary work carried out in Phase-1 during the previous semester.

3.15.4 The Project Report/Thesis / Dissertation report / Drawings prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

3.15.5 The deadline for submission of final Project Report / Thesis / Dissertation is within 30 calendar days from the last working day of the semester in which Project / Thesis / Dissertation is done.

3.15.6 If a student fails to submit the Project Report / Thesis / Dissertation on or before the specified deadline he / she is deemed to have not completed the Project Work / Thesis / dissertation and shall re-register the same in a subsequent semester.

4.0 CLASS ADVISOR AND FACULTY ADVISOR

4.1 Class Advisor

A faculty member will be nominated by the HOD as Class Advisor for the whole class.

He / she is responsible for maintaining the academic, curricular and co-curricular records of all students throughout their period of study.

4.2 Faculty Advisor

To help the students in planning their courses of study and for general counseling on the academic programme, the Head of the Department of the students will attach a certain number of students to a faculty member of the department who shall function as Faculty Advisor for the students throughout their period of study. Such Faculty Advisor shall offer advice to the students on academic and personal matters and guide the students in taking up courses for registration and enrolment every semester.

5.0 CLASS COMMITTEE

5.1 Every class of the PG Programme will have a Class Committee constituted by the Head of the Department as follows:

i. Teachers of all courses of the programme

ii. One senior faculty preferably not offering courses for the class, as Chairperson.

iii. Minimum two students of the class, nominated by the Head of the Department.

iv. Class Advisor / Faculty Advisor of the class - Ex-Officio Member

v. Professor in-charge of the PG Programme - Ex-Officio Member.

5.2 The Class Committee shall be constituted by the respective Head of the Department of the students.

5.3 The basic responsibilities of the Class Committee are to review periodically the progress of the classes to discuss problems concerning curriculum and syllabi and the conduct of classes. The type of assessment for the course will be decided by the teacher in consultation with the Class Committee and will be announced to the students at the beginning of the semester. Each Class Committee will communicate its recommendations to the Head of the Department and Dean (Academic Affairs). The class committee, **without the student members,** will also be responsible for finalization of the semester results and award of grades.

5.4 The Class Committee is required to meet at least thrice in a semester, first within a week of the commencement of the semester, second, after the first assessment and the third, after the semester-end examination to finalize the grades.

6.0 COURSE COMMITTEE

Each common theory course offered to more than one group of students shall have a “Course Committee” comprising all the teachers teaching the common course with one of them nominated as Course coordinator. The nomination of the Course coordinator shall be made by the Head of the Department / Dean (Academic Affairs) depending upon whether all the teachers teaching the common course belong to a single department or to several departments. The Course Committee shall meet as often as possible and ensure uniform evaluation of the tests and arrive at a common scheme of evaluation for the tests. Wherever it is feasible, the Course Committee may also prepare a common question paper for the test(s).

7.0 REGISTRATION AND ENROLMENT

7.1 For the first semester every student has to register for the courses within one week from the commencement of the semester

7.2 For the subsequent semesters registration for the courses will be done by the student one week before the last working day of the previous semester. The curriculum gives details of the core and elective courses, project and seminar to be taken in different semester with the number of credits. The

student should consult his/her Faculty Advisor for the choice of courses. The Registration form shall be filled in and signed by the student and the Faculty Advisor.

7.3 From the second semester onwards all students shall pay the prescribed fees and enroll on a specified day at the beginning of a semester.

7.4 A student will become eligible for enrolment only if he/she satisfies clause 9 and in addition he/she is not debarred from enrolment by a disciplinary action of the Institution. At the time of enrolment a student can drop a course registered earlier and also substitute it by another course for valid reasons with the consent of the Faculty Advisor. Late enrolment will be permitted on payment of a prescribed fine up to two weeks from the date of commencement of the semester.

7.5 Withdrawal from a course registered is permitted up to one week from the date of the completion of the first assessment test.

7.6 Change of a course within a period of 15 days from the commencement of the course, with the approval of Dean (Academic Affairs), on the recommendation of the HOD, is permitted.

7.7 Courses withdrawn will have to be taken when they are offered next if they belong to the list of core courses.

7.8 A student undergoing a full time PG Programme should have enrolled for all preceding semesters before registering for a particular semester

7.9 A student undergoing the P.G. programme in Part Time mode can choose not to register for any course in a particular semester with written approval from the head of the department. However the total duration for the completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1)

8.0 TEMPORARY BREAK OF STUDY FROM THE PROGRAMME

A student may be permitted by the Dean (Academic Affairs) to avail temporary break of study from the programme up to a maximum of two semesters for reasons of ill health or other valid grounds. Such student has to rejoin only in the same semester from where he left. However the total duration for completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1).

9.0 MINIMUM REQUIREMENTS TO REGISTER FOR PROJECT / THESIS / DISSERTATION

9.1 A student is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	Minimum No. of credits to be earned to enroll for project semester
M. Tech. (Full time / Part time)	18
M.C.A. (Full time / Part time)	45
M.C.A. (Full time / Part time) – (Lateral Entry)	22
M.Sc.(Full time / Part time)	18

9.2 If the student has not earned minimum number of credits specified, he/she has to earn the required credits, at least to the extent of minimum credits specified in clause 9.1 and then register for the project semester.

10.0 DISCIPLINE

10.1 Every student is required to observe discipline and decorous behavior both inside and outside the campus and not to indulge in any activity, which will tend to bring down the prestige of the Institution.

10.2 Any act of indiscipline of a student reported to the Head of the Institution will be referred to a Discipline and Welfare Committee for taking appropriate action.

11.0 ATTENDANCE

11.1 Attendance rules for all Full Time Programme and Part time Programmes are given in the following sub-clause.

11.2 Ideally every student is expected to attend all classes and earn 100% attendance in the contact periods of every course, subject to a maximum relaxation of 25% for genuine reasons like on medical grounds, representing the University in approved events etc., to become eligible to appear for the semester-end examination in that course, failing which the student shall be awarded "I" grade in that course. If the course is a core course, the student should register for and repeat the course when it is offered next. If the course is an elective, either he/she can register and repeat the same elective or can register for a new elective.

11.3 The students of Full Time mode of study, who have not attended a single hour in all courses in a semester and awarded ‘I’ grade are not permitted to

write the examination and also not permitted move to next higher semester. Such students should repeat all the courses of the semester in the next Academic year.

12.0 SUMMER TERM COURSES

12.1 Summer term courses may be offered by a department on the recommendation of the Departmental Consultative Committee and approved by the Dean (Academic Affairs). No student should register for more than three courses during a summer term.

12.2 Summer term courses will be announced by the Head of the department at the end of the even semester before the commencement of the end semester examinations. A student will have to register within the time stipulated in the announcement. A student has to pay the fees as stipulated in the announcement.

12.3 The number of contact hours and the assessment procedure for any course during summer term will be the same as those during regular semesters.

Students with U grades will have the option either to write semester end arrears exam or to redo the courses during summer / regular semesters, if they wish to improve their continuous assessment marks subject to the approval of the Head of the department.

12.4 Withdrawal from a summer term course is not permitted. No substitute examination will be conducted for the summer term courses.

12.5 The summer term courses are not applicable for the students of Part Time mode.

13.0 ASSESSMENTS AND EXAMINATIONS

13.1 The following rule shall apply to all the PG programmes (M. Tech. / M.C.A. / M.Sc.)

For lecture-based courses, normally a minimum of two assessments will be made during the semester. The assessments may be combination of tests and assignments. The assessment procedure as decided in the Class Committee will be announced to the students right from the beginning of the semester by the course teacher.

13.2 There shall be one examination of three hours duration, at the end of the semester.

13.3 In one (or) two credit courses that are not spread over the entire semester, the evaluation will be conducted at the completion of the course itself. Anyhow approval for the same is to be obtained from the HoD and the Dean of Academic Affairs.

13.4 The evaluation of the Project work will be based on the project report and a Viva-Voce Examination by a team consisting of the supervisor concerned, an Internal Examiner and External Examiner to be appointed by the Controller of Examinations.

13.5 At the end of industrial internship, the student shall submit a certificate from the organization and also a brief report. The evaluation will be made based on this report and a Viva-Voce Examination, conducted internally by a Departmental Committee constituted by the Head of the Department.

14.0 WEIGHTAGES

14.1 The following shall be the weightages for different courses:

i) Lecture based course

Two continuous assessments	50%
Semester-end examination	50%

ii) Laboratory based courses

Laboratory work assessment	75%
Semester-end examination	25%

iii) Project work

Periodic reviews	50%
Evaluation of Project Report by	
External Examiner	20%
Viva-Voce Examination	30%

14.2 Appearing for semester end examination for each course (Theory and Practical) is mandatory and a student should secure a minimum of 40% marks in semester end examination for the successful completion of the course.

14.3 The markings for all tests, tutorial, assignments (if any), laboratory work and examinations will be on absolute basis. The final percentage of marks is calculated in each course as per the weightages given in clause 13.1.

15.0 SUBSTITUTE EXAMINATION

15.1 A student who has missed for genuine reasons any one of the three assessments including semester-end examination of a course may be permitted to write a substitute examination. However, permission to take up a substitute examination will be given under exceptional circumstances, such as accident or admissions to a hospital due to illness, etc.

15.2 A student who misses any assessment in a course shall apply in a prescribed form to the Dean (Academic Affairs) through the Head of the department within a week from the date of missed assessment. However

the substitute tests and examination for a course will be conducted within two weeks after the last day of the semester-end examinations.

16.0 COURSEWISE GRADING OF STUDENTS AND LETTER GRADES

16.1 Based on the semester performance, each student is awarded a final letter grade at the end of the semester in each course. The letter grades and the corresponding grade points are as follows, but grading has to be relative grading

Letter grade	Grade points
S	10
A	9
B	8
C	7
D	6
E	5
U	0
W	-
I	-
AB	-

- Flexible range grading system will be adopted
- **“W”** denotes withdrawal from the course.
- **"I"** denotes inadequate attendance and hence prevention from semester-end examination
- **"U"** denotes unsuccessful performance in a course.
- **“AB”** denotes absent for the semester end examination

16.2 A student is considered to have completed a course successfully if he / she secure five grade points or higher. A letter grade ‘U’ in any course implies unsuccessful performance in that course.

16.3 A course successfully completed cannot be repeated for any reason.

17.0 AWARD OF LETTER GRADE

17.1 A final meeting of the Class Committee without the student member(s) will be convened within ten days after the last day of the semester end examination. The letter grades to be awarded to the students for different courses will be finalized at the meeting.

17.2 After finalization of the grades at the class committee meeting the Chairman will forward the results to the Controller of Examinations, with copies to Head of the Department and Dean (Academic Affairs).

18.0 DECLARATION OF RESULTS

18.1 After finalization by the Class Committee as per clause 16.1 the Letter grades awarded to the students in the each course shall be announced on the departmental notice board after duly approved by the Controller of Examinations.

18.2 In case any student feels aggrieved about the results, he/she can apply for revaluation after paying the prescribed fee for the purpose, within one week from the announcement of results.

A committee will be constituted by the concerned Head of the Department comprising of the Chairperson of the concerned Class Committee (Convener), the teacher concerned and a teacher of the department who is knowledgeable in the concerned course. If the Committee finds that the case is genuine, it may jointly revalue the answer script and forward the revised marks to the Controller of Examinations with full justification for the revision, if any.

18.3 The “U” and “AB” grade once awarded stays in the grade sheet of the students and is not deleted when he/she completes the course successfully later. The grade acquired by the student later will be indicated in the grade sheet of the appropriate semester.

19.0 COURSE REPETITION AND ARREARS EXAMINATION

19.1 A student should register to re-do a core course wherein "I" or "W" grade is awarded. If the student is awarded "I" or "W" grade in an elective course either the same elective course may be repeated or a new elective course may be taken.

19.2 A student who is awarded “U” or “AB” grade in a course shall write the semester-end examination as arrear examination, at the end of the next semester, along with the regular examinations of next semester courses.

19.3 A student who is awarded “U” or “AB” grade in a course will have the option of either to write semester end arrear examination at the end of the subsequent semesters, or to redo the course whenever the course is offered. Marks earned during the redo period in the continuous assessment for the course, will be used for grading along with the marks earned in the end-semester (re-do) examination.

19.4 If any student obtained “U” or “AB” grade, the marks earned during the redo period for the continuous assessment for that course will be considered for

further appearance as arrears.

19.5 If a student with "U" or "AB" grade prefers to redo any particular course fails to earn the minimum 75% attendance while doing that course, then he/she will not be permitted to write the semester end examination and his / her earlier 'U' grade and continuous assessment marks shall continue.

20.0 GRADE SHEET

20.1 The grade sheet issued at the end of the semester to each student will contain the following:

(i) the credits for each course registered for that semester.

(ii) the performance in each course by the letter grade obtained.

(iii) the total credits earned in that semester.

(iv) the Grade Point Average (GPA) of all the courses registered for that semester and the Cumulative Grade Point Average (CGPA) of all the courses taken up to that semester.

20.2 The GPA will be calculated according to the formula

$$GPA = \frac{\sum_{i=1}^{n}(C_i)(GP_i)}{\sum_{i=1}^{n}(C_i)}$$

where n = number of courses

where C_i is the number of credits assigned for i^{th} course

GP_i - Grade point obtained in the i^{th} course

for the cumulative grade point average (CGPA) a similar formula is used except that the sum is over all the courses taken in all the semesters completed up to the point of time.

'I' and 'W' grades will be excluded for GPA calculations.

'U', 'AB' 'I' and 'W' grades will be excluded for CGPA calculations.

20.3 Classification of the award of degree will be as follows:

20.3.1 For students under full time mode of study

CGPA	Classification
8.50 and above, having completed all courses in first appearance	First class with Distinction
6.50 and above, having completed within a period of 2 semesters beyond the programme period	First Class
All others	Second Class

However, to be eligible for First Class with Distinction, a student should not have obtained U or I grade in any course during his/her study and should have completed the PG Programme within a minimum period covered by the minimum duration (clause 3.1) plus authorized break of study, if any (clause 8). To be eligible for First Class, a student should have passed the examination in all courses within the specified minimum number of semesters reckoned from his/her commencement of study plus two semesters. For this purpose, the authorized break of study will not be counted. The students who do not satisfy the above two conditions will be classified as second class. For the purpose of classification, the CGPA will be rounded to two decimal places. For the purpose of comparison of performance of students and ranking, CGPA will be considered up to three decimal places.

20.3.2 For students under part time mode of study

CGPA	Classification
8.50 and above, having completed all courses in first appearance	First class with Distinction
6.50 and above	First Class
All others	Second Class

For the purpose of classification, the CGPA will be rounded to two decimal places.

21.0 ELIGIBILITY FOR THE AWARD OF THE MASTERS DEGREE

21.1 A student shall be declared to be eligible for the award of the Masters Degree, if he/she has:

i) successfully acquired the required credits as specified in the Curriculum corresponding to his/her programme within the stipulated time,

ii) no disciplinary action is pending against him/her.

21.2 The award of the degree must be approved by the University.

22.0 POWER TO MODIFY

Notwithstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

CURRICULUM & SYLLABI FOR

M. Tech. (VLSI &Embedded Systems)
(FOUR SEMESTERS / FULL TIME)

CURRICULUM

Sl. No.	Course Code	Course Title	L	T	P	C
		SEMESTER I				
1	MAC6184	Probability Matrix Theory & Linear Programming	**3**	**1**	**0**	**4**
2	ECC6121	Advanced Embedded System	**3**	**0**	**0**	**3**
3	ECC6122	Digital VLSI Design	**3**	**0**	**2**	**4**
4	ECC6123	Advanced Microcontroller architecture and Programming	**3**	**0**	**2**	**4**
5	ECC6124	Embedded System Lab	**0**	**0**	**2**	**1**
6		Professional Elective (Minimum of 3 credits to be earned)				**3**
						19
		SEMESTER II				
1	GEC6201	Research Methodology for Engineers	**3**	**0**	**0**	**3**
2	ECC6221	ASIC Design	**3**	**0**	**0**	**3**
3	ECC6222	Real Time Operating Systems	**3**	**0**	**0**	**3**
4	ECC6223	Analog Integrated Circuit Design	**3**	**0**	**2**	**4**
5	ECC6224	VLSI Physical Design Automation Lab	**0**	**0**	**2**	**1**
6		Professional Elective (Minimum of 9 credits to be earned)				**9**
						23

Sl. No.	Course Code	Course Title	L	T	P	C
		SEMESTER III				
1		General Elective	**3**	**0**	**0**	**3**
2	ECC7121	Project Work - Phase I	**0**	**0**	**12**	**6***
3	ECC7122	Mini Project/Internship	**0**	**0**	**2**	**1**
4		Professional Elective (Minimum of 6 credits to be earned)				**6**
						10
		SEMESTER IV				
1	ECC7121	Project Work - Phase II	**0**	**0**	**36**	**18***
						18 + 6 = 24

* Credits for Project Work Phase I to be accounted along with Project Work Phase II in IV Semester

Total Credits: 76

LIST OF PROFESSIONALELECTIVES

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECCY009	Internet of Things	**3**	**0**	**0**	**3**
2	ECCY040	Advanced Digital System Design	**3**	**0**	**0**	**3**
3	ECCY041	CAD for VLSI Circuits	**3**	**0**	**0**	**3**
4	ECCY042	CMOS Mixed Signal Circuit Design	**3**	**0**	**0**	**3**
5	ECCY043	Control Area Network	**3**	**0**	**0**	**3**
6	ECCY044	Distributed Embedded Computing	**3**	**0**	**0**	**3**
7	ECCY045	Embedded Networking	**3**	**0**	**0**	**3**
8	ECCY046	Embedded LINUX	**3**	**0**	**0**	**3**
9	ECCY047	Hardware-software co-design	**3**	**0**	**0**	**3**
10	ECCY048	IC packaging and Interconnects	**3**	**0**	**0**	**3**
11	ECCY049	Low Power VLSI Design	**3**	**0**	**0**	**3**
12	ECCY050	MEMS System Design	**3**	**0**	**0**	**3**
13	ECCY051	Optimization Techniques and their applications in VLSI design	**3**	**0**	**0**	**3**
14	ECCY052	Programming Verilog HDL	**2**	**0**	**2**	**3**
15	ECCY053	Real Time Systems	**3**	**0**	**0**	**3**
16	ECCY054	Reconfigurable Computing	**3**	**0**	**0**	**3**
17	ECCY055	RF Integrated Circuits Design	**3**	**0**	**0**	**3**
18	ECCY056	RISC Processor Architecture and Programming	**3**	**0**	**0**	**3**
19	ECCY057	Semiconductor Memories	**3**	**0**	**0**	**3**
20	ECCY058	Signal integrity for high speed design	**3**	**0**	**0**	**3**
21	ECCY059	SoC design and Verification	**3**	**0**	**0**	**3**
22	ECCY060	Software for Embedded Systems	**2**	**0**	**2**	**3**

Sl. No.	Course Code	Course Title	L	T	P	C
23	ECCY061	Testing of VLSI Circuits	**3**	**0**	**0**	**3**
24	ECCY062	VLSI Digital Signal Processing	**3**	**0**	**0**	**3**
25	ECCY063	WSN Architecture and Programming	**3**	**0**	**0**	**3**
26	ECCY064	DSP System Design	**2**	**0**	**0**	**2**
27	ECCY065	Electronic Design Automation Tools	**2**	**0**	**0**	**2**
28	ECCY066	Programming System Verilog	**2**	**0**	**0**	**2**
29	ECCY067	Sensors Lab	**0**	**0**	**2**	**1**
30	ECCY068	Scripting Languages for VLSI Design Automation	**1**	**0**	**0**	**1**
31	EIC6212	Industrial Automation using PLC, DCS and SCADA	**3**	**0**	**2**	**4**
32	MACY081	Signal Processing Techniques	**3**	**1**	**0**	**4**

GENERAL ELECTIVES FOR M.TECH PROGRAMMES

Sl. No.	Course Code	Course Title	L	T	P	C
1	GECY101	Project Management	**3**	**0**	**0**	**3**
2	GECY102	Society, Technology & Sustainability	**3**	**0**	**0**	**3**
3	GECY103	Artificial Intelligence	**3**	**0**	**0**	**3**
4	GECY104	Green Computing	**3**	**0**	**0**	**3**
5	GECY105	Gaming Design	**3**	**0**	**0**	**3**
6	GECY106	Social Computing	**3**	**0**	**0**	**3**
7	GECY107	Soft Computing	**3**	**0**	**0**	**3**
8	GECY108	Embedded System Programming	**3**	**0**	**0**	**3**
9	GECY109	Principles of Sustainable Development	**3**	**0**	**0**	**3**
10	GECY110	Quantitative Techniques in Management	**3**	**0**	**0**	**3**
11	GECY111	Programming using MATLAB & SIMULINK	**1**	**0**	**2**	**2**
12	GECY112	JAVA Programming	**1**	**0**	**2**	**2**
13	GECY113	PYTHON Programming	**1**	**0**	**2**	**2**
14	GECY114	Intellectual Property Rights	**1**	**0**	**0**	**1**

SEMESTER I

		L	T	P	C
MAC6184	**PROBABILITY, MATRIX THEORY AND LINEAR PROGRAMMING**	**3**	**1**	**0**	**4**

OBJECTIVE:

The aim of this course is to

- Provide a comprehensive introduction to the probability distributions used in engineering.
- Familiarize students with advanced matrix theory and variational problems.
- Expose the students to Operations Research using concepts of linear programming.

MODULE I PROBABILITY DISTRIBUTIONS (10+03)

Axioms of probability – addition and multiplication theorem – conditional probability – total probability – random variables - moments – moments generating functions and their properties- Binomial, Poisson, Geometric, Uniform, Exponential and Normal distributions.

MODULE II TWO DIMENSIONAL RANDOM VARIABLES (08+03)

Joint distributions - marginal and conditional distributions - functions of random variables - covariance - correlation and regression - Central limit theorem.

MODULE III ADVANCED MATRIX THEORY (09+03)

Matrix norms - singular value decomposition - QR algorithm - Pseudo inverse - Least square approximations.

MODULE IV LINEAR PROGRAMMING (10+03)

Formation - graphical method - simplex method - Big-M method - Two Phase method - transportation and assignment problems.

MODULE V CALCULUS OF VARIATIONS (08+03)

Variation and its properties – Euler's equation – functional dependant on first and higher order derivatives – functional dependant on functions of several independent variables – variational problems with moving boundaries – isoperimetric problems – Ritz and Kantorovich methods.

L – 45; T – 15; Total – 60

TEXT BOOKS:

1. S.M.Ross, “A First Course in Probability”, 9th edition, Pearson Education, 2013.
2. Lewis.D.W., “Matrix Theory”, Allied Publishers, Chennai, 1995.
3. Taha, H.A., “Operations Research - An Introduction ", 10th edition, Pearson Prentice Hall, 2016.
4. A.S. Gupta, “Calculus of variations with applications”, PHI Pvt. Ltd, New Delhi, 2011.

REFERENCES:

1. H. Cramer., “Random Variables and Probability Distributions”, Cambridge University Press (2004).
2. Roger A. Horn, Charles R. Johnson, “Matrix Analysis”, Cambridge University Press; 2nd edition (2012).
3. Robert.J.Vanderbei., “Linear Programming: Foundations and Extensions”, Springer US(2014).
4. David. J. Rader., “Deterministic Operations Research”, Wiley (2010).
5. Elsgolts, “Differential Equations and Calculus of Variations", University Press of the Pacific (2003).

OUTCOMES:

At the end of the course students will be able to

- Solve problems using concept of standard, discrete and continuous distributions.
- Solve problems using one dimensional and two dimensional random variables.
- Find Eigen values and Eigen vectors of a higher order matrix.
- Solve problems of linear programming.
- Solve problems of calculus of variations by direct methods and using Euler’s formulae.

ECC6121 ADVANCED EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To explore Embedded system lifecycle
- To Introduce the occurrence of shared data problem in embedded systems
- To describe need for power management techniques in embedded systems
- To familiarize the debugging in embedded systems

MODULE I EMBEDDED DESIGN LIFE CYCLE 09

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking –RTOS Micro Controller – RTOS availability – Tool chain availability – Other issues in selection processes..

MODULE II EMBEDDED HARDWARE AND SOFTWARE 09

Review of basics in embedded hardware and software– Hardware software co design- Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency – Interrupt routines in an RTOS environment – Hard Real Time scheduling considerations - Embedded platform boot sequence.

MODULE III MEMORY AND INTERFACING 09

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing - communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access– Arbitration -Multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols

MODULE IV INTEGRATION AND TESTING OF EMBEDDED HARDWARE AND FIRMWARE 09

Integration of Hardware and Firmware-In system programming-The Integrated development environment-Debugging techniques- Host based debugging – Remote debugging – ROM emulators – Logic analyzer- Real time trace – Hardware break points – Overlay memory- Testing embedded software

MODULE V POWER OPTIMIZATION TECHNIQUES IN EMBEDDED SYSTEMS 09

The power profile of an Embedded Computing Systems – Constant versus Dynamic power – A simple model of power efficiency – Advanced Configuration and Power Interface – ACPI system states- Case Study- power optimization techniques in wireless sensor networks.

Total Hours: 45

REFERENCES:

1. Arnold S. Berger – “Embedded System Design: An introduction to processor, tools and techniques”, CMP books, USA, 2002.
2. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.
3. Frank Vahid and Tony Givargis ‘Embedded Systems Design: A Unified Hardware/Software Introduction’, John & Wiley Publications, 2002.
4. Peter Barry, Patrick Crowley, “Modern Embedded Computing” Morgan Kaufmann Publishers, 2012.

OUTCOMES:

On completion of program students will be able to

- Analyze the quality principles and tools in embedded system during product development process
- Analyze the division of hardware/software in embedded systems.
- Develop the interrupt routines in RTOS environment
- Design energy efficient embedded systems
- Design interface circuit with processor and peripheral devices
- Test and debug the coding in embedded systems

ECC6122 DIGITAL VLSI DESIGN

L	T	P	C
3	0	2	4

OBJECTIVES:

The objective of the course is

- To learn the fundamentals of digital CMOS VLSI design from the transistor up to the system level.
- To introduce the models for state-of-the-art VLSI components, fabrication steps, hierarchical design flow and semiconductor business economics.
- To design full custom digital integrated circuits

MODULE I MOS TRANSISTOR INTRODUCTION AND CMOS LOGIC 09+06

MOS Device Physics, MOS Models, MOS Device Design Equations Device Scaling & Short-channel effects Layout & Design Rules, CMOS Logic, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Switch Models & Simple RC Models, Power, Energy, and Energy Delay parameters.

Laboratory Practice: Circuit Simulation of CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates.

MODULE II COMBINATIONAL, SEQUENTIAL AND DYNAMIC LOGIC CIRCUITS 11+06

Pass Transistors, Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.SR Latch, clocked Latch and flip flop circuits, CMOS D-latch and edge triggered flip flop. Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

Laboratory Practice: Circuit Simulation of Dynamic CMOS design- Domino and NORA logic – Flip flop -RS, D, JK, MS, T

MODULE III CMOS SUB SYSTEM DESIGN 09+06

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

Laboratory Practice: Circuit Simulation of Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter –CMOS memory design - SRAM and DRAM

MODULE IV INTERCONNECT &TIMING METRICS 09+06

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design, Synchronizers and Arbiters, Clock Synthesis and Synchronization Using Phase-Locked Loop

Laboratory Practice: Circuit Simulation of the worst-case propagation delay of static and dynamic logic circuits

MODULE V SYSTEMS DESIGN AND DESIGN METHOD 07+06

Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing -Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.

Laboratory Practice: Simulation and synthesis of Serial & Parallel adder using HDL Test bench and interpretation of synthesis report of EDA tools

L: 45, P:30 - Total Hours: 75

REFERENCES

1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective” 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2nd edn., Pearson Education, 2003. ISBN: 8178089912
3. Wayne, Wolf, “Modern VLSI design: System on Silicon” Pearson Education”, Second Edition
4. John P. Uyemura, “CMOS Logic Circuit Design”, Springer (Kluwer Academic Publishers), 2001.
5. Ken Martin, “Digital Integrated Circuit Design”, Oxford University Press, 2000
6. Douglas A Pucknell & Kamran Eshragian, “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

7. Sung Mo Kang &Yosuf Lederabic Law, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill (Third Edition)

OUTCOMES:

On completion of program students will be able to

- Describe the MOS transistor characteristics and simple device models
- Design, simulate and analyze CMOS inverter characteristics.
- Design, simulate and analyze static and dynamic logic circuits
- Evaluate the timing performance of digital circuits.
- Design and analyze data path architectures.
- Discuss the digital system design process and verification methods

ECC6123	ADVANCED MICROCONTROLLER ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	2	4

OBJECTIVES:

- To know Microcontroller based system design, applications.
- To teach I/O interface in system Design
- To learn about Design and programming of MSP 430 microcontroller
- To involve the students to Practice on Workbench /Software Tools/ Hardware Processor Boards with the supporting Peripherals

MODULE I 8051 MICROCONTROLLER ARCHITETURE 09+06

Architecture – memory organization – addressing modes – instruction set-I/O programming-Timer programming – Serial port programming-Interrupt programming

Laboratory Practice: Practice in 8051 microcontroller based assembly/C language programming-I/O programming -Timer Counter Programming – Serial Communication- practice in KEIL µvision IDE complier

MODULE II PIC MICROCONTROLLER ARCHITETURE 09+06

Architecture – memory organization – addressing modes – instruction set : arithmetic, logic instruction, branch, call, and time delay loop–I/O ports-bank switching, table processing, macros and modules.

Laboratory Practice: Practice on PIC Microcontroller based Assembly/C language programming – Arithmetic Programming- practice in MPLAB compiler

MODULE III PIC PROGRAMMING IN ASSEMBLY AND C 09+06

I/O programming-Timer programming – Serial port programming-Interrupt programming-ADC, DAC and Sensor interfacing- Flash and EEPROM memories-I2C bus-CCP and ECCP programming-Practice in MPLAB

Laboratory Practice: Practice on PIC Microcontroller based Assembly/C language programming – Timer Counter Programming – Serial Communication-Programming Interrupt - practice in MPLAB compiler

MODULE IV MSP430 architecture and programming 09+06

Architecture – CPU features – Memory structure - Addressing modes – Instruction sets Interrupts programming– Input and Output programming– On-chip peripherals– Hardware considerations – Flash memory – Low power design- Practice in IAR workbench

Laboratory Practice: Practice on MSP430 Microcontroller based Assembly/C language I/O programming – Timer Counter Programming – Serial Communication- Programming Interrupt - practice in IAR workbench compiler

MODULE V SYSTEM DESIGN – CASE STUDY 09+06

Interfacing LCD Display – Keypad Interfacing - Motor Control – Controlling DC/ AC appliances – Measurement of frequency - Stand-alone Data Acquisition System.

Laboratory Practice: Design a mini project using PIC or MSP430

L: 45, P: 30 - Total Hours: 75

REFERENCES:

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey “PIC Microcontroller and Embedded Systems using Assembly and C for PIC18”, Pearson Education 2008
2. John Iovine, “PIC Microcontroller Project Book”, McGraw Hill 2000
3. Rajkamal, “Microcontrollers Architecture, Programming”, Interfacing, & System Design”,Pearson,2012
4. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier 2003.

OUTCOMES:

On completion of the course the students will be able to

- Describe the architecture of PIC series of microcontroller
- Create ALP and C programs to develop applications using 8051 & PIC microcontroller
- Describe the architecture of MSP series of microcontroller
- Create ALP and C programs to develop applications using the MSP microcontroller
- Interface the internal and External IOs of PIC and MSP microcontroller.
- Use KEIL µvision IDE,IAR Embedded workbench and MPLAB IDE

ECC6124 EMBEDDED SYSTEMS LAB

L	T	P	C
0	0	2	1

OBJECTIVES:

- To gain knowledge in programming with software tools and microcontrollers with peripheral interfaces.
- To develop a program and simulate 8, 16 and 32 bit microcontrollers in both assembly and C programming.
- To learn programming with sensors
- To focus on the embedded system hardware development

LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers- Assembly and C Programming: I/O Programming, Timers.
2. Interrupts, Serial port programming with 8051/PIC Microcontrollers- Assembly and C programming.
3. PWM Generation, Motor Control, ADC/DAC with 8051/PIC Microcontrollers- Assembly and C programming.
4. LCD and RTC Interfacing, Sensor Interfacing with 8051/PIC Microcontrollers- Assembly and C programming
5. Design with 16 bit processors: I/O programming, Timers, Interrupts, Serial Communication
6. Design with ARM Processors: I/O programming, ADC/DAC, Timers, Interrupts
7. Study of one type of Real Time Operating Systems (RTOS)
8. Mini-project

P: 30 - Total Hours:30

OUTCOMES:

On completion of program students will be able to

- Simulate simple application programs through Keil µ vision.
- Interface I/O ports, timers, seven segments LED, serial ports with 8051/ PIC Microcontrollers.
- Demonstrate programming with sensors
- Employ Assembly language and C programming to verify the stepper motor and real time clock interface.
- Develop a real time embedded applications using 8051and PIC Microcontrollers.
- Appraise a real time operating system.

SEMESTER II

GEC6201	RESEARCH METHODOLOGY FOR ENGINEERS	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objective of the course is

- To provide a perspective on research to the scholars
- To educate on the research conceptions for designing the research
- To impart knowledge on statistical techniques for hypothesis construction
- To gain knowledge on methods of data analysis and interpretation
- To learn about the effective communication of research finding

MODULE I RESEARCH PROBLEM FORMULATION 07

Research – objectives – types, Research process, Solving engineering problems, Identification of research topic, Formulation of research problem, Literature survey and review.

MODULE II HYPOTHESIS FORMULATION 08

Research design – meaning and need – basic concepts, Different research designs, Experimental design – principle – important experimental designs, Design of experimental setup, Mathematical modeling, Simulation – validation and experimentation, Dimensional analysis and similitude.

MODULE III STATISTICAL TECHNIQUES 12

Statistics in research – concept of probability – popular distributions –Hypothesis testing- sample design- Design of experiments – factorial designs -– orthogonal arrays- ANOM - ANOVA - Multivariate analysis - Use of optimization techniques – traditional methods – evolutionary optimization techniques –Transportation model

MODULE IV STATISTICAL ANALYSIS OF DATA 10

Research Data analysis – interpretation of results – correlation with scientific facts- Accuracy and precision – error analysis, limitations - Curve fitting, Correlation and regression.

MODULE V RESEARCH REPORT 08

Purpose of written report – audience, synopsis writing, preparing papers for International journals, Thesis writing – organization of contents – style of writing – graphs and charts – referencing, Oral presentation and defence, Ethics in research, Patenting, Intellectual Property Rights

L: 45 - Total Hours: 45

REFERENCES

1. Ganesan R., Research Methodology for Engineers, MJP Publishers, Chennai, 2011.
2. Ernest O., Doebelin, Engineering Experimentation: planning, execution, reporting, McGraw Hill International edition, 1995
3. George E. Dieter., Engineering Design, McGraw Hill – International edition, 2000
4. Madhav S. Phadke, Quality Engineering using Robust Design, Printice Hall, Englewood Cliffs, New Jersey, 1989.
5. Kothari C.R., Research Methodology – Methods and Techniques, New Age International (P) Ltd, New Delhi, 2003.
6. Kalyanmoy Deb., “Genetic Algorithms for optimization”, KanGAL report, No.2001002
7. Holeman, J.P., Experimental methods for Engineers, Tata McGraw Hill Publishing Co., Ltd., New Delhi, 2007.
8. Govt. of India, Intellectual Property Laws; Acts, Rules & Regulations, Universal Law Publishing Co. Pvt. Ltd., New Delhi 2010.
9. University of New South Wales, “How to write a Ph.D. Thesis” Sydney, Australia, Science @ Unsw.
10. Shannon. R.E., System Simulation: the art and science, Printice Hall Inc, Englewood Cliffs, N.J.1995.
11. Scheffer. R.L. and James T. Mc Clave, Probability and Statistics for Engineers, PWS – Kent Publishers Co., Boston, USA, 1990.

OUTCOMES:

Students should be able to

- Formulate the research problem
- Design and Analyse the research methodology
- Construct and optimize the research hypothesis
- Analyse and interpret the data
- Report the research findings

ECC6221 ASIC DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to impart knowledge on

- The concept of structure and features of full custom and semicustom ASIC types.
- The fundamentals of digital logic design and the physical features of each ASIC.
- ASIC logic design, testing of physical design partitioning, floor planning, placement and routing.

MODULE I INTRODUCTION TO ASICs, ASIC LIBRARY DESIGN 09

Types of ASICs - Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design.

MODULE II PROGRAMMABLE ASICs AND LOGIC CELLS 09

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III INTERCONNECTS AND LOW LEVEL DESIGN LANGUAGES 09

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language .

MODULE IV LOGIC SYNTHESIS, SIMULATION AND TESTING 09

Verilog and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

MODULE V PARTITIONING, FLOOR PLANNING, PLACEMENT & ROUTING 09

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

L: 45 - Total Hours: 45

REFERENCES

1. H. Bhatnagar, “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time”, 2nd edition, 2001
2. M.J.S .Smith, "Application Specific Integrated Circuits ", Addison -Wesley Longman Inc., 2003.
3. Keith Barr “ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits”,McGrawHill,2006
4. Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991

OUTCOMES:

At the end of the course the students will be able to

- Describe ASIC Design Flow and its Architecture.
- Describe the Logic Synthesis and Testing methodologies
- Architect ASIC library design
- Develop programmable ASIC logic cells
- Design I/O cells and interconnects
- Identify new developments in SOC

ECC6222 REAL TIME OPERATING SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to

- Introduce the concepts of Operating systems and Real-time Operating Systems
- Impart knowledge on Resource management, time-constrained communication, scheduling and imprecise computations, real-time kernels and case studies.
- Compare various RTOS.

MODULE I REVIEW OF OPERATING SYSTEMS 09

Basic Principles - Operating System structures – System Calls – Files –Concurrent Execution & Interrupts- Processes – Design and Implementation of processes – Communication between processes-Process Scheduling.

MODULE II OVERVIEW OF RTOS 09

Real-time System: Hard versus Soft Real-time systems – examples-Difference between Traditional OS and RTOS. RTOS Kernel -RTOS Task and Task state Multitasking – Task Assignment, Task Priorities, Scheduling.

MODULE III IPC MECHANISMS 09

Intertask Communication & Synchronization – Definition of Context Switching, Critical Section – Re-entrant Functions, Deadlocks, Interprocess Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, and Message Queues.

MODULE IV REAL TIME MODELS AND LANGUAGES 09

Event Based – Process Based and Graph based Models – Real Time Languages – RT scheduling -Interrupt processing -Control Blocks – Memory Requirements.

MODULE V REAL TIME KERNEL AND RTOS APPLICATION 09

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – µC/OS-II – RT Linux Case studies-RTOS for fault Tolerant Applications – RTOS for Control Systems.

L: 45 - Total Hours: 45

REFERENCES

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
2. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
3. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
4. Charles Crowley, “Operating Systems-A Design Oriented approach” Tata McGraw Hill.

OUTCOMES:

After successful completion of the course, the students shall be able to

- Illustrate OS structure and explain process scheduling types.
- Compare the features of traditional OS and RTOS.
- Describe inter task communication and synchronization mechanisms.
- Analyze and design real time scheduling algorithms
- Select appropriate RTOS for the required application.
- Determine the common faults that occur in RTOS based embedded system.

ECC6223 ANALOG INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	0	2	4

OBJECTIVES:

The objective of the course is to

- Introduce the principles of analog circuits and apply the techniques for the design of analog integrated circuit
- Analysis, design, and applications of modern analog circuits using CMOS technologies.
- Analysis of basic Multipliers, wave shaping circuits and basic operation of PLL.
- Implement a complete analog system.

MODULE I INTRODUCTION 09

Analog MOS transistor models Temperature effects and Noise in MOS transistor MOS resistors, characterization of resistive, capacitive elements and MOS devices. Passive and active CMOS current sink/ sources. Effects due to nonlinearity and mismatch in MOS circuits.

Laboratory Practice

Verification of MOS Device Characterization and parametric (PAR) analysis, Current Mirrors: Simple, cascode, feedback and low-voltage

MODULE II SINGLE STAGE CMOS AMPLIFIERS 09

Basics of single stage CMOS amplifiers - common Source, common gate and source follower. Frequency response of common Source, common gate and source follower.

Laboratory Practice

Simulation of Single stage Amplifiers-Diode connected, Current Mirror Load, PMOS with self biased load and self biased CMOS.

MODULE III CMOS DIFFERENTIAL AMPLIFIERS 09

CMOS Operational Amplifiers one stage and two stage gain boosting Common mode feedback (CMFB) Cascode and Folded cascade structures.

Laboratory Practice: Differential Amplifiers: Simple and cascode current mirrors.

MODULE IV HIGH PERFORMANCE OP-AMPS 09

High speed/ high frequency op-amps, micro power op-amps, low noise op-amps and low voltage op-amps. Current mirrors filter implementations. Supply

independent and temperature independent references Band gap references PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits .

Laboratory Practice

Operational Trans-conductance Amplifiers (OTA), Two stage OP-AMP.

MODULE V SWITCHED CAPACITOR CIRCUITS 09

First and Second Order Switched Capacitor Circuits, Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs non ideal effects in PLLs, Delay locked loops, frequency locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.

Laboratory Practice

Verification of switched capacitor Integrators.

L:45, L:30 - Total Hours:75

REFERENCES

1. David. A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2001.
2. BehzadRazavi, “Design of Analog CMOS Integrated Circuit”, Tata McGraw HILL, 2002.
3. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002.
4. Mohammed Ismail &Feiz, “Analog VLSI – Signal Information and Processing”, John Wiley and Sons.

OUTCOMES:

After successful completion of the course, the students shall be able to

- Characterize the MOSFET and perform parametric analysis for the simple MOS models.
- Analyze and design MOSFET based Amplifier circuits.
- Design and analyze band gap reference biasing sources.
- Design and analyze operational amplifier circuits
- Design and analyze switched capacitor based mixed signal circuits
- Use the Composer (schematic capture), Virtuoso (layout generation), Spectre HDL (circuit simulation), Diva tools (DRC, LVS, ERC, extraction) tools for designing analog integrated circuits.

ECC6224	VLSI PHYSICAL DESIGN AUTOMATION LAB	L	T	P	C
		0	0	2	1

OBJECTIVES:

The objective of the course is to

- Make the students capable to design FPGA based digital systems
- Analyze the performance of the digital systems using EDA Tools
- Impart hands-on experience on the VLSI physical design tools.

FPGA Based Experiments

1. Design Entry of Verilog examples using HDL languages sequential and concurrent statements.
2. Data path and Controller architecture Verilog examples of sequential & combinational circuits, Test vector generation.
3. Verilog examples for FPGA Implementation, I/O devices interfacing
4. Verilog examples illustrating Static and dynamic power Analysis-Xilinx ISE / Quartus
5. Verilog examples illustrating Static and dynamic Timing analysis procedures and constraints, Critical path considerations –. Xilinx ISE / Quartus
6. Designing FIR filter using Xilinx ISE System Generator and MATLAB simulink

ASIC Based Experiments

7. ASIC RTL realization using standard cell libraries- Cadence/Tanner/Mentor Graphics.
8. Static and dynamic power Analysis- Cadence/Tanner/Mentor Graphics.
9. Static and dynamic Timing analysis procedures and constraints.
10. Critical path considerations – Cadence/Tanner/Mentor Graphics.
11. Layout design, LVS, Back annotation- Cadence/TANNER/ Mentor Graphics

P: 30 - Total Hours:30

OUTCOMES:

After successful completion of the course, the students shall be able to

- Design digital circuits using verilog HDL
- Estimate and analyze the static and dynamic power of a digital system using EDA tools

- Estimate and analyze the timing performance of a digital system using EDA tools
- Develop digital systems meeting the functionality ,timing and power constraints using EDA tools
- Design layouts and schematic of digital circuit using EDA tools
- Work in projects involving the design of digital ICs

SEMESTER-III

		L	T	P	C
ECC7121	**PROJECT WORK – PHASE I**	**0**	**0**	**12**	**6**

OBJECTIVES :

- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice of students
- To apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

GUIDELINES:

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least four faculty members of which internal guide and other experts in the specified area of the project shall be two essential members.

OUTCOMES:

At the end of the project work phase I the student will be able to

- learn the tool required for the design, analysis of their preliminary work
- Select the specific devices for different application along with justification
- Apply the practical knowledge while solving real time problems
- Incorporate cost effective and efficient project models
- Conclude the subject knowledge through proto type models
- Prepare an appropriate documentation

ECC7122	MINI PROJECT	L	T	P	C
		0	0	2	1

OBJECTIVES :

- To improve the professional competency and research aptitude of students

GUIDELINES:

1. This mini project will help the students to develop the work practice to apply the design skills for solving real life problems.
2. The project can be an experimental project on any of the topics in electronics and communication.
3. The project work is allotted individually on different topics.
4. The students shall be encouraged to do their project in the parent institute itself.
5. Department will constitute an Evaluation Committee to review the project periodically.

OUTCOMES:

At the end of the project the student will be able to

- Design and analyze an electronic system
- Fabricate an electronic system/device in their area of interest
- Improve their presentation skills
- Improve the documentation skills

SEMESTER-IV

		L	T	P	C
ECB7121	**PROJECT WORK – PHASE II**	**0**	**0**	**36**	**18**

OBJECTIVES:

- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

GUIDELINES:

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least four faculty members of which internal guide and other experts in the specified area of the project shall be two essential members.

OUTCOMES:

- At the end of the project work student will be able to use the theoretical and practical tools/techniques to solve real life problems related to industry and current research problems.

PROFESSIONAL ELECTIVES

ECCY009	INTERNET OF THINGS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce emerging technological options and platforms
- To explain the architecture of IoT
- To explore application development for mobile Platforms
- To Provide the appropriate IoT solutions and recommendations according to the applications used.

MODULE I THE IOT NETWORKING CORE 10

History of IoT, Review of Technologies involved in IoT Development, Internet/Web and Networking Basics -OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing. Basics of Big Data, Data Science.

MODULE II IOT ARCHITECTURE AND APPLICATIONS 09

Architecture: M2M – Machine to Machine, Web of Things, IoT protocol, Introduction to wireless and mobile networks, ZigBee, BLE mesh, WiFi, MQTT, LoRa-Machine Applications: Remote Monitoring & Sensing, Remote Controlling, Performance Analysis

MODULE III IOT PLATFORM OVERVIEW 09

Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.

MODULE IV IOT APPLICATION DEVELOPMENT 09

Application Protocols-MQTT, REST/HTTP, CoAP, MySQL -Back-end Application - Design Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS &jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application

Development for mobile Platforms: Overview of Android / IOS 10 25 47 /97 App Development tools

MODULE V CASE STUDY & ADVANCED IOT APPLICATIONS 08

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards

L:45, T:15 - Total Hours:60

REFERENCES

1. Jean-Philippe Vasseur, Adam Dunkels, “Interconnecting Smart Objects with IP: The Next Internet”, Morgan Kuffmann-2010
2. Vijay Madisetti , Arshdeep Bahga, : Internet of Things (A Hands-on-Approach)” -2014
3. Adrian McEwen (Author), Hakim Cassimally, “Designing the Internet of Things” ,Wiley -2013
4. Dr. OvidiuVermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems,” River Publishers -2013
5. Barrie Sosinsky, “Cloud Computing Bible”, Wiley-India, 2010
6. Asoke K Talukder and Roopa R Yavagal, “Mobile Computing,” Tata McGraw Hill, 2010.
7. Adelstein and S.K.S. Gupta, “Fundamentals of Mobile and Pervasive Computing,” McGraw Hill, 2009
8. Ronald L. Krutz, Russell Dean Vines “Cloud Security: A Comprehensive Guide to Secure Cloud Computing”, Wiley-India, 2010

OUTCOMES:

At the end of the course the student will be able to

- Articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art Internet of things
- Identify the architecture and infrastructure of IoT.
- Explain the core issues of IoT such as security, privacy, and interoperability
- Choose the appropriate technologies, algorithms, and approaches for the related issues.
- Identify problems, and explain, analyze, and evaluate various IoT solutions
- Attempt to generate new ideas and innovations in IoT.

ECCY040 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To provide knowledge to design sequential and asynchronous sequential circuit.
- To introduce programmable logic devices and its application to circuit design
- To introduce the concepts involved in designing fault free circuits.

MODULE I SEQUENTIAL CIRCUIT DESIGN 09

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modelling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits, Design of Arithmetic circuits for Fast adder- Array Multiplier- Verilog design of clocked synchronous sequential circuits

MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 09

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC using ASM charts – Derivation of SM charts, and Realization of SM charts.– Static and Dynamic Hazards – Essential Hazards – Designing vending Machine Controller – Mixed Operating Mode Asynchronous Circuits-Verilog design of Asynchronous sequential circuits

MODULE III DESIGNING WITH PROGRAMMABLE LOGIC DEVICES 09

ROM- Internal ROM structure – Implementation of Boolean functions using ROM-Design of Sequential circuits using ROM, PROM – Realization State machine using PLD, PAL, PLA, Programmable Gate Arrays, Programmable Logic sequencer, Field Programmable Gate Array Families. Verilog design of programmable logic devices

MODULE IV FAULT DIAGONOSIS AND TESTING 09

Fault detection and location, gate sensitivity, path sensitization, undetectable faults, bridging fault, two level circuit fault detection, Boolean difference -D algorithm - Tolerance techniques, compact testing technique; scan path testing, design for testability.

MODULE V SYSTEM DESIGN USING VERILOG 09

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

L:45 - Total Hours:45

REFERENCES

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2002.
2. Stephen Brown and ZvonkVranesic, “Fundamentals of Digital Logic with Verilog Design”, Tata McGraw Hill, 2002.
3. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
4. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 1999
5. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson , 2003.

OUTCOMES:

After successful completion of the course, the students will be able to

- To analyze clocked synchronous sequential circuits and design digital systems based on the given specifications.
- To analyze asynchronous sequential circuits and design digital systems based on the given specifications.
- To make state machines and ASM charts for the given design requirements.
- To select and use appropriate PLDs to realize digital systems based on the requirements.
- To perform fault diagnosis and testing in digital circuit
- To apply the digital system design principles and make projects based on the requirements.

ECCY041 CAD FOR VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to impart knowledge on

- The principles of operation of all the important modules that go into the construction of a complete VLSI CAD tool
- The standard cell based synthesis methodologies for digital VLSI.
- The floor planning and placement principles and related topics
- To use Computer Aided Design (CAD) VLSI design tools.

MODULE I VLSI DESIGN METHODOLOGIES 09

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Introduction to CAD tools - Evolution of Design Automation-Basic Transistor Fundamentals-CMOS realizations of basic gates - Modeling techniques, Types of CAD tools.

MODULE II PARTITIONING 09

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - partitioning Classification of Partitioning Algorithms - Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning

MODULE III FLOOR PLANNING 09

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

MODULE IV PLACEMENT 09

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement, Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing

MODULE V MODELING AND SYNTHESIS 09

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem -

High level transformations. Introduction to Reconfigurable computing, FPGAs, the Altera Quartus II flow.

L:45 - Total Hours:45

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002..
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Samir Palnitkar, “Verilog HDL”, Second Edition, Pearson Education, 2004.
4. J.Bhaskar, “Verilog HDL Synthesis”, BS publications, 2001.

OUTCOMES:

On completion of the course the students will be able to

- Discuss the operation of complete VLSI CAD tool
- Perform high level synthesis
- Discuss floor planning concepts
- Design algorithms for placement and partitioning
- Develop hardware models and synthesis algorithms for VLSI CAD tools
- Use VLSI design automation tools

ECCY042 CMOS MIXED SIGNAL CIRCUIT DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To know different mixed-signal circuit design methodologies.
- To acquire knowledge on design of sampling circuits and integrator.
- To discuss different design architectures in mixed signal mode.
- To gain knowledge on filter design in mixed signal mode.

MODULE I PLL AND SWITCHED CAPACITOR CIRCUITS 09

Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

MODULE II SAMPLING CIRCUITS 09

Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, openloop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

MODULE III DAC 09

Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

MODULE IV ADC 09

Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures,

pipelined architectures, Successive approximation architectures, interleaved architectures.

MODULE V FILTERS 09

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and bi-quadratic transfer function.

L:45 - Total Hours:45

REFERENCES

1. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, 2001.
2. Razavi, “Principles of data conversion system design”, S.Chand and company ltd, 2000.
3. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2002.
4. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 1987.
5. Baker Li, Boyce, “CMOS: Circuit Design, layout and Simulation”, PHI, 2000.

OUTCOMES:

On completion of the course the students will be able to

- Describe the models for PLL circuits
- Summarize the low-voltage, low-power design techniques for mixed-signal CMOS ICs.
- Analyze CMOS based switched capacitor circuits.
- Design non-linear analog circuits and data converters.
- Design and analyze comparators, sample and hold circuits, switched capacitor circuits.
- To design and implement filters

ECCY043 CONTROL AREA NETWORK

L	T	P	C
3	0	0	3

OBJECTIVES:

The primary course objectives are

- To introduce the requirements of embedded networking
- To provide overview of CAN controller and its implementation.
- To explain CAN open configuration and its development tools.

MODULE I EMBEDDED NETWORK REQUIREMENTS 09

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

MODULE II CAN OPEN 09

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

MODULE III CAN 09

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

MODULE IV IMPLEMENTATION OF CAN OPEN 09

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle, CAN Bus Analyzer.

MODULEV ISSUES 09

Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

L: 45 - Total Hours:45

REFERENCES

1. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.

2. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2005.
3. Mohammed Farsi, Barbosa, “CANopen Implementation : Applications to Industrial Network (Industrial Control, Computers, and Communications Series,18),Research Studies Press,2000
4. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2007

OUTCOMES:

On completion of the course the students will be able to

- Demonstrate embedded networking and its requirements.
- Describe CAN controller.
- Interpret the CAN message format.
- Determine system requirements for choosing devices and tools
- Implement CAN and discuss CAN issues.
- Explain different types of noise commonly found in embedded networks.

ECCY044 DISTRIBUTED EMBEDDED COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

The primary course objectives are

- The various hardware and software architectures used for distributed embedded computing.
- Distributed computing system models and Distributed databases.
- The infrastructure required to support an Internet connection, uses of common Internet protocols, and basic principles of the DNS.
- The distributed computing technologies.

MODULE I THE HARDWARE INFRASTRUCTURE 09

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – wide Area Networks – Network management – Network Security – Cluster computers.

MODULE II INTERNET CONCEPTS 09

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

MODULE III DISTRIBUTED COMPUTING USING JAVA 09

I/O streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

MODULE IV EMBEDDED AGENT 09

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

MODULE V EMBEDDED COMPUTING ARCHITECTURE 09

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

L:45 - Total Hours:45

REFERENCES

1. Dietel&Dietel, “JAVA-How to program”, Prentice Hall 1999.
2. SapeMullender, “Distributed Systems”, Addison-Wesley, 1993.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
4. Bernd Kleinjohann “Architecture and Design of Distributed Embedded Systems”, C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

OUTCOMES:

On completion of the course the students will able to

- Describe the hardware infra structure of distributed embedded system
- Elucidate the architecture of embedded web server
- Create JAVA constructs for distributed computing
- Designing and analyze high-performance Embedded system
- Analyze the performance of multiprocessor system on chip architecture
- Select suitable embedded architecture for distributed embedded system

ECCY045 EMBEDDED NETWORKING

L	T	P	C
3	0	0	3

OBJECTIVES:

The primary course objectives are

- To study the concepts of embedded networking
- To explore various bus architectures.
- To explore the fundamentals of embedded security.

MODULE I THE AUTOMOTIVE CAN BUS 09

Introduction-Concepts of Bus Access and arbitration – error processing and management – definition of the CAN protocol ISO 11898-1-error properties-detection and processing – framing, signal propagation-Bit synchronization-high speed CAN – low speed CAN-CAN components and development tools for CAN.

MODULE II UNIVERSAL SERIAL BUS 06

USB bus –Introduction –Speed Identification on the bus – USB States –USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface –C Programs

MODULE III INDUSTRIAL NETWORKING PROTOCOL 09

LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audio-video buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'- profi bus

MODULE IV ETHERNET BASICS 06

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

MODULE V BLUETOOTH AND ZIGBEE 09

Bluetooth: Specifications- Bluetooth Radio- Type of Antenna, Antenna Parameters-Bluetooth Networking- Connection establishment procedure, Profile and usage model - Wireless networking, wireless network types, devices roles and states – IEEE 802.15.4 –Zigbee specifications- Zigbee stack protocol stack-PAN formation.

MODULE V IRF COMMUNICATION 06

Adhoc network, scatter net- GSM- Overview of IrDA, Home RF, Wireless LANs- IEEE 802.11x - NFC (near-field communication)- Wireless sensor networks – Introduction – Applications.

L: 45 - Total Hours:45

REFERENCES

1. Dominique Paret,"Multiplexed Networks for Embedded Systems", Wiley 2007.
2. Jan Axelson, "USB Complete", Lakeview Research, 2005
3. Jan Axelson, "Embedded Ethernet Complete", Lakeview Research, 2005.
4. GlafP.Feiffer, Andrew Ayre and Christian Keyold, "Embedded networking with CAN and CAN open". Embedded System Academy 2005.
5. Gregory J. Pottie, William J. Kaiser "Principles of Embedded Networked Systems Design", Cambridge University Press, Second Edition, 2005.
6. C.S.R. Prabhu and A.P. Reddi ,"Bluetooth Technology and its Applications with JAVA and J2EE, PHI, 2006
7. Rappaport Theodore S, "Wireless Communications: Principles And Practice", Pearson Education, 2010
8. Shahin Farahani,"ZigBee Wireless Networks and Transceivers", Newnes Publications, 2008.

OUTCOMES:

On completion of the course the students will able to:

- Describe the components and significance of Embedded networking system
- Elucidate the principles of USB communications
- Create Embedded Ethernet controller
- Explain industrial networking protocols like I2C,D2B
- Use appropriate interfaces, protocols and buses in embedded systems
- Describe the architecture of Bluetooth and RF communication modules

ECCY046 EMBEDDED LINUX

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To learn fundamentals of embedded linux.
- To familiarize the use of GNU tool chain.
- To develop embedded applications in linux platform.
- To interface peripheral devices in Linux platform.

MODULE I LINUX FUNDAMENTALS 09

Introduction - host-target development setup - hardware support -development languages and tools – RT Linux.

MODULE II KERNEL INITIALIZATION 09

Linux kernel and kernel initialization - system initialization – hardware support - boot loaders.

MODULE III DEVICE HANDLING 09

Device driver basics - module utilities - file systems - MTD subsystems –busy box

MODULE IV DEVELOPMENT TOOLS 09

Embedded development environment - GNU debugger - tracing & profiling tools - binary utilities - kernel debugging - debugging embedded Linux applications - porting Linux - Linux and real time - SDRAM interface.

MODULE V DEVICE APPLICATIONS 09

Asynchronous serial communication interface - parallel port interfacing -USB interfacing - memory I/O interfacing - using interrupts for timing.

L:45 - Total Hours:45

REFERENCES:

1. Karim Yaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, “Building embedded linux systems”, O'Reilly, 2008.
2. Christopher Hallinan, “Embedded Linux Primer: A practical real world approach”, Prentice Hall, 2007.

3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton, 2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

OUTCOMES

At the end of the course students will be able to

- Explain RT linux fundamentals
- Identify difference between RT linux and embedded linux versions
- Analyze kernel and system initialization and porting Linux
- Debug and develop embedded linux applications
- Interface peripheral devices in linux platform
- Explain device handling in linux OS.

ECCY047 HARDWARE-SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to

- Introduce the basics of hardware software Co-design.
- Describe the modeling concepts in Co-design.
- Explain the applications of models.
- Apply object oriented techniques in Co-Design process.

MODULE I INTRODUCTION 09

Motivation hardware & software co-design, system design consideration, research scope & overviews Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development

MODULE II CO-DESIGN CONCEPTS 09

Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software tradeoffs, co-design.

MODULE III METHODOLOGY FOR CO-DESIGN 09

Amount of unification, general consideration & basic philosophies, a framework for co-design Unified Representation for Hardware & Software: Benefits of unified representation, modeling concepts. An Abstract Hardware & Software Model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model Performance Evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation

MODULE IV OBJECT ORIENTED TECHNIQUES IN HARDWARE DESIGN 09

Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, and Processor example.

MODULE V SYSTEM ON CHIP 09

The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

L:45 - Total Hours:45

REFERENCES

1. Sanjaya Kumar, James H. Ayler “The Co-design of Embedded Systems: A Unified Hardware Software Representation”, Kluwer Academic Publisher, 2002 .
2. H. Kopetz, “Real-Time Systems”, Kluwer, 1997.
3. R. Gupta, “Co-synthesis of Hardware and Software for Embedded Systems”, Kluwer 1995.
4. S. Allworth, “Introduction to Real-time Software Design”, Springer-Verlag, 1984.
5. C. M. Krishna, K. Shin, “Real-time Systems”, Mc-Graw Hill, 1997.
6. Peter Marwedel, G. Goosens, “Code Generation for Embedded Processors”, Kluwer Academic Publishers, 1995.
7. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998

OUTCOMES:

At the end of the course students will be able to

- Describe the design methodologies used in the hardware software co-design
- Identify the core issues in co-design
- Describe the functions of co-design
- Assess the benefits of unified representation
- Evaluate the performance of the model
- Apply object oriented techniques in Hardware Design

ECCY048 IC PACKAGING AND INTERCONNECTS

L	T	P	C
3	0	0	3

OBJECTIVES:

- Outline packaging techniques and materials used for packaging.
- Understanding the assembly process in electronic design.
- Design PCB for various applications
- Testing and interconnections of electronic modules.

MODULE I PACKAGING TECHNIQUES 09

Introduction to packaging, Package design considerations, VLSI Assembly Techniques, Packaging fabrication technology, THM, Surface Mounting.

MODULE II SYSTEM ASSEMBLY 09

Design for Reliability – Fundamentals, Induced failures. IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging.

MODULE III INTERCONNECTS 09

Small, Intermediate and long interconnects in VLSI, Interconnect Parasitics: Resistance, Inductance and Capacitance. Interconnect RC Delays: Elmore Delay Calculation. Interconnect Models: Lumped RC Model, Distributed RC Model, Transmission line model. SPICE Wire Models: Distributed RC lines in SPICE, Transmission line models in SPICE.

MODULE IV CMOS REPEATER DRIVEN INTERCONNECTS 09

The Static Behavior-Switching Threshold, Noise Margins, The Dynamic Behavior-Computing the capacitances, Propagation Delay: First order Analysis, Propagation Delay from a Design perspective. Power, energy and Energy – Delay-Dynamic Power Consumption, Static Consumption, Transient analysis of repeater loaded interconnects and analysis of Power Consumption using SPICE

MODULE V ADVANCED INTERCONNECT TECHNIQUES 09

Reduced - swing Circuits, Current – mode Transmission Techniques, Clocking of high - speed systems, CNT and Optical Interconnects.

L: 45 - Total Hours:45

REFERENCES

1. Rao R. Tummala : Fundamentals of Microsystem Packaging McGraw Hill.
2. H.K. Bakoglu, “Circuits, Interconnections & Packaging for VLSI”, Addison Wesley Publication Company Inc.
3. Richard K. Ulrich &William D. Brown “Advanced Electronic Packaging” - 2nd Edition : IEEE Press
4. A.K. Goel, High-Speed VLSI Interconnections, Wiley Interscience, 2nd Edition, 2007.

OUTCOMES:

At the end of the course students will be able to

- Describe the different types IC packaging techniques
- Describe the multidisciplinary aspects of IC packaging like electrical, thermal, material, reliability and testability design.
- Model the interconnects inside the IC using suitable models
- Analyze the performance of the Interconnects using SPICE
- Analyze the performance of the CMOS driven interconnects.
- Describe the advanced Interconnect Techniques

ECCY049 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

To impart knowledge on

- Power analysis used in CMOS devices.
- Various techniques to reduce the power consumption in VLSI Circuits.
- Various Low power Architectures.
- Algorithm and Architecture level methodologies on low power devices.

MODULE I DEVICE & TECHNOLOGY IMPACT ON LOW POWER 09

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

MODULE II SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS 09

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation -Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

MODULE III LOW POWER DESIGN 09

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre computation logic.

MODULE IV LOW POWER ARCHITECTURE SYSTEMS & CLOCK DISTRIBUTION 09

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design, Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co-design of clock network.

MODULE V ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES 09

Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis.

L: 45 - Total Hours:45

REFERENCES

1. Gary K. Yeap, Farid N. Najm, “Low power VLSI design and technology”, World Scientific Publishing Ltd., 1996.
2. DimitriosSoudris, Christian Piguet, Costas Goutis, “Designing CMOS circuits for low power”, Kluwer Academic Publishers, 2002
3. Kaushik Roy and Sharat C. Prasad, “Low-Power CMOS VLSI Circuit Design”, Wiley-Interscience, 2000.
4. Chandrakasan, R. Brodersen, “CMOS Low Power Digital Design”, Kluwer Academic Publications, 1995.
5. Rabaey, M. Pedram, “Low Power Design Methodologies”, Kluwer Academic Publications, 1996.
6. Christian Piguet, “Low-power CMOS circuits: technology, logic design and CAD tools”, CRC Press, Taylor & Francis Group, 2006.

OUTCOMES:

After successful completion of the course, the students will be able to

- Describe the static and dynamic power dissipation in integrated chips.
- Estimate the power for simple models.
- Apply low power dissipation techniques in Clocking strategies and I/O circuits.
- Design low power arithmetic circuits and systems.
- Analyze design chips used for battery-powered systems and high-performance circuits not exceeding the power limits.
- Decide at which level of abstraction it is advantageous to implement low power techniques in a VLSI system design

ECCY050 MEMS SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to

- Provide the basic of MEMS device fabrication
- Fulfill the need of electronic engineer who wants to create MEMS devices
- Introduce the concepts of MEMS Electronic Sensors, Optical and RF system

MODULE I INTRODUCTION TO MEMS 09

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication.

MODULE II MECHANICS FOR MEMS DESIGN 09

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics - actuators, force and response time, Fracture and thin film mechanics.

MODULE III ELECTRO STATIC DESIGN 09

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators

MODULE IV CIRCUIT AND SYSTEM ISSUES 09

Electronic Interfaces, Feedback systems, Noise , Circuit and system issues, Case studies - Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

MODULE V INTRODUCTION TO OPTICAL AND RF MEMS 09

Optical MEMS - System design basics - Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS - design basics, case study - Capacitive RF MEMS switch, performance issues.

L:45 - Total Hours:45

REFERENCES:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000.
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton, 2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

OUTCOMES

At the end of the course students will be able to

- Describe the process of MEMS fabrication
- Describe the mechanisms followed to design MEMS devices
- Elucidate the methods to make electrostatic MEMS sensors
- Elucidate the methods to make MEMS based accelerometers
- Describe the MEMS based RF Switches
- Discuss the MEMS based optical scanners and sensors

ECCY051	OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objective of the course is

- To introduce the concepts of statistical modeling and test generation patterns
- To describe and analyze placement and power estimation
- To discuss about various convex optimization techniques
- To gain knowledge in fundamentals of generic algorithms

MODULE I STATISTICAL MODELING 07

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

MODULE II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS 07

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

MODULE III CONVEX OPTIMIZATION 08

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Max- monomial fitting, Posynomial fitting.

MODULE IV GENETIC ALGORITHM 08

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic Placement, Routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding- local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

MODULE V GENETIC ENCODING 07

Hybrid genetic-genetic encoding- Local Improvement - WDFR- Comparison of Gas- Standard cell Placement- GASP Algorithm- Unified Algorithm.

MODULE VI GA ROUTING PROCEDURES AND POWER ESTIMATION 08

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function- GA vs Conventional algorithm.

L:45 - Total Hours:45

REFERENCES

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI: Timing and Power”, Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design, Layout and test Automation”, Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University Press, 2004.

OUTCOMES:

On completion of the course the students will be able to

- Apply Knowledge on basic optimization techniques.
- Select and implement appropriate formulations and algorithms.
- Develop the capability to analyze on various statistical methods in analyzing a Sample.
- Develop the capability to analyze the concepts of genetic algorithms and genetic encoding.
- Apply engineering tools and techniques to conduct engineering VLSI design.
- To adopt these techniques in solving problems in the real world.

ECCY052 PROGRAMMING VERILOG HDL

L	T	P	C
2	0	2	3

OBJECTIVES:

The primary course objectives is to

- Learn the hardware description language Verilog HDL.
- Learn the hardware description language Verilog AMS
- Become proficient in a design methodology that uses Verilog HDL to create and verify systems implemented using PLDs
- Strengthen and extend your understanding of the theory and fundamentals of digital system design.

MODULE I VERILOG HDL INTRODUCTION 06+06

Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Language Constructs and Conventions, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators. Modeling at Dataflow Level, Continuous Assignment Structure, Delays Assignment to Vector, Operators

Laboratory Practice

Simulation of Verilog HDL programs illustrating the language constructs in the module I

MODULE II GATE LEVEL MODELING 06+06

Modeling at Gate Level, Gate Primitives, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Switch Level Modeling, Basic Transistor Switches, CMOS Switches, Bi-Directional Gates, Time Delays with Switch Primitives, Instantiation with 'Strengths' and 'Delays' Strength Contention with Trireg Nets.

Laboratory Practice

Simulation of Verilog HDL programs illustrating the language constructs in the module II

MODULE III BEHAVIORAL MODELING 06+06

Functional Bi-furcation, 'Intial' and ‘always’ Construct, 'Wait' Construct, Multiple ‘always’ Block, Designsat Behavioral Level, Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If' an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable'

Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event. System Tasks, Functions and Compiler Directives, Path Delays, Module Parameters. System Tasks and Functions File Based Tasks and Functions, Computer Directives, Hierarchical Access, User Defined Primitives.

Laboratory Practice

Simulation of Verilog HDL programs illustrating the language constructs in the module III

MODULE IV SEQUENTIAL CIRCUIT DESCRIPTION 06+06

Basic Memory Components, Functional Register, Finite State Machine Coding, Sequential Synthesis. Components Test and Verification: Test Bench - Combinational Circuits Testing, Sequential Circuit Testing, Test Bench Techniques, Design Verification, Assetion Verification.

Laboratory Practice

Simulation of Verilog HDL programs illustrating the language constructs in the module IV

MODULEV VERILOG-AMS 06+06

Introduction to Verilog-AMS: Verilog Family of Languages Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior.

Laboratory Practice

Simulation of Verilog AMS HDL programs illustrating the language constructs in the module V

L: 30, P: 30 - Total Hours:60

REFERENCES

1. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.
2. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI, 2009.
5. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004

OUTCOMES:

On completion of the course the students will be able to

- Differentiate sequential language and concurrent language

- Design and verify combinational logic circuits using Verilog HDL
- Design and verify sequential logic circuits using Verilog HDL
- Implement RTL models on FPGAs
- Model Analog circuits using Verilog AMS.
- Design digital and mixed signal systems using Verilog HDL

ECCY053 REAL TIME SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To know the fundamentals of Real Time systems
- To know the concepts related to Scheduling and Programming Languages
- To describe of real time database and communication
- To understand fault tolerance and techniques

MODULE I INTRODUCTION TO REAL TIME SYSTEM 09

Introduction – characterizing real time system -Performance Measures for Real Time Systems – Estimating Program Run Times – Task Assignment and Scheduling.

MODULE II PROGRAMMING LANGUAGES AND TOOLS 09

Desired language characteristics – Data typing – Control structures – Facilitating Hierarchical Decomposition, Packages, Run time Error handling – Overloading and Generics – Multitasking – Timing Specifications – Programming Environments – Run time support.

MODULE III REAL TIME DATABASES 09

Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

MODULE IV REAL TIME COMMUNICATION 09

Communications media, Network Topologies, Protocols- contention based, Token based, Stop-and-Go multihop, Polled Bus, Hierarchical Round Robin Protocol, Deadline-Based Protocols, Fault Tolerant Routing.

MODULE V FAULT TOLERANT AND EVALUATION TECHNIQUES 09

Fault Tolerance Techniques – Fault Types – Fault Detection-Fault Error containment- Redundancy- Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy – Software error models.

L: 45 - Total Hours:45

REFERENCES

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 1997
2. Rajib Mall, ”Real-time systems: theory and practice”, Pearson Education, 2007
3. Stuart Bennett, “Real Time Computer Control – An Introduction”, Prentice Hall of India, 1998.
4. Peter D. Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.
5. S.T. Allworth and R.N.Zobel, “Introduction to real time software design”, Macmillan

OUTCOMES:

At the end of the course students will be able to

- Describe the characteristics of real time system
- Apply scheduling algorithms based on application
- Analyze real-time systems designs
- Identify the fault tolerants in real time system
- Apply reliable evaluation techniques
- Design the real time systems

ECCY054 RECONFIGURABLE COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To investigate the state-of-the-art in reconfigurable computing both from a hardware and software perspective.
- To make the students understand both how to architect a reconfigurable systems and how to apply them to solving challenging computational problems.
- To examine specific contemporary reconfigurable computing systems and to identify existing system limitations and to highlight opportunities for research in dynamic and partial configuration areas.
- To impart knowledge on the application development of reconfigurable systems.

MODULE I INTRODUCTION 09

Introduction, origin of reconfigurable computing, Reconfigurable computing architecture, Reconfigurable computing hardware, Logic—The Computational Fabric, The Array and Interconnect, Extending Logic, Configuration, Case Studies, Altera Stratix, Xilinx Virtex-II Pro.

MODULE II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 09

Reconfigurable Processing Fabric Architectures, RPF Integration into Traditional Computing Systems, Reconfigurable computing systems, Early Systems, PAM, VCC, and Splash , Small-scale Reconfigurable Systems, Circuit Emulation, Accelerating Technology, Reconfigurable Supercomputing, Other System Issues, The Future of Reconfigurable Systems.

MODULE III PROGRAMMING RECONFIGURABLE SYSTEMS, COMPUTATION MODELS AND SYSTEM ARCHITECTURES 09

Computation Models -- Challenges, Common Primitives, Dataflow, Sequential Control, Data Parallel, Data-centric , Multi-threaded, Other Compute Models, System Architectures - Streaming Dataflow, Sequential Control, Bulk Synchronous Parallelism, Data Parallel, Cellular Automata, Multi-threaded, Hierarchical Composition.

MODULE IV FPGA DESIGN 09

FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

MODULE V APPLICATION DEVELOPMENT 09

Implementing Applications with FPGAs, Strengths and Weaknesses of FPGAs, Application Characteristics and Performance, General Implementation Strategies for FPGA-based Systems, Implementing Arithmetic in FPGAs, Hardware/Software Partitioning.

L:45 - Total Hours:45

REFERENCES

1. Scott Hauck, André DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation”, Morgan Kauffman publishers, 2008.
2. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
3. C. Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2007.
4. P. Lysaght and W. Rosenstiel, “New Algorithms, Architectures and Applications for Reconfigurable Computing”, Springer, 2005.
5. W. Wolf, “FPGA Based System Design”, Prentice-Hall, 2004.

OUTCOMES:

After successful completion of the course, the students will be able to

- Describe various Reconfigurable Computing architectures systems
- Summarize the Programming model for Reconfigurable computing
- Design reconfigurable computing architectures on FPGA
- Apply Reconfigurable computing for hardware and software partitioning.
- Design and build an SOPC for a specific application.
- Develop arithmetic and complex digital architectures on FPGA

ECCY055 RF INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to impart knowledge on

- The different RF transceiver architectures
- The methods of designing passive components in IC
- The design of LNA, Power amplifiers, PLL, Oscillators and frequency synthesizers

MODULE I TRANSCEIVER ARCHITECTURES 09

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures upconversion Transmitter.

MODULE II IMPEDANCE MATCHING AND AMPLIFIERS 09

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs. MOSFET amplifier controlled by AGC.

MODULE III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 09

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MODULE IV PLL AND FREQUENCY SYNTHESIZERS 09

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer- N frequency synthesizers, Direct Digital Frequency synthesizers.

MODULE V MIXERS AND OSCILLATORS 09

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers,

Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

L: 45 - Total Hours:45

REFERENCES

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

OUTCOMES:

After successful completion of the course, the students will be able to

- Describe and select appropriate RF transceiver architectures based on the requirements.
- Describe the different topologies used to design passive components in IC
- Analyze Low Noise and power amplifier circuits and design the same based on the given requirements.
- Describe and analyze the performance of frequency synthesizers
- Analyze mixers and oscillator circuits and design the same based on the given requirements.
- Design the building blocks of RF transceiver system

ECCY056	RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objective of the course is to

- Compare CISC and RISC processor architectures
- Understand AVR microcontroller architecture and memory organization
- Introduce MSP430 processor architecture and programming
- Familiarize ARM architecture ,application and programming

MODULE I AVR MICROCONTROLLER ARCHITECTURE 09

Architecture – memory organization – addressing modes – instruction set – programming techniques –Assembly language & C programming-Development Tools – Cross Compilers – Hardware Design Issues.

MODULE II MSP430 ARCHITECTURE AND PROGRAMMING 09

Architecture – CPU features – Memory structure - Interrupts – Input and Output– On-chip peripherals – Addressing modes – Instruction sets – Hardware considerations – Flash memory – Programming in Low power design.

MODULE III ARM ARCHITECTURE AND PROGRAMMING 09

ARM processor fundamentals – Registers – Pipeline – Exceptions – Interrupts– core extension- Instruction set – Thumb instruction set - 'C' programming –writing and optimising ARM assembly code – Instruction scheduling – Register allocation – conditional execution – Looping constraints.

MODULE IV ARM APPLICATION DEVELOPMENT 09

Exception Handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Example: Standalone - Embedded Operating Systems –Fundamental Components - Example Simple little Operating System.

MODULE V DESIGN WITH ARM MICROCONTROLLERS 09

Integrated development environment – Standard I/O Libraries - User Peripheral Devices – Application of ARM processor: Wireless Sensor Networks.

L: 45 - Total Hours:45

REFERENCES:

1. Dananjay V. Gadre “Programming and Customizing the AVR microcontroller”,McGrawHill 2001
2. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier 2003.
3. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier, 2007.
4. Steve Furber, “ARM system on chip architecture”, Addison Wesley, 2000.

OUTCOMES

On completion of program students will be able to:

- Analyze the features of CISC and RISC processor architectures
- Develop simple application program using AVR microcontroller
- Integrate low power modes with embedded system application
- Implement scheduling mechanism in ARM processor.
- Use simple little operating system for suitable applications.
- Estimate energy consumption of ARM processor in wireless sensor network

ECCY057 SEMICONDUCTOR MEMORIES

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To study the concepts of random access memory and nonvolatile memories.
- To learn the implementation methods and problems in designing and making semiconductor memories
- To understand different fault modeling and testing techniques.

MODULE I STATIC RANDOM ACCESS MEMORY TECHNOLOGY 09

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAM

MODULE II DYNAMIC RANDOM ACCESS MEMORY TECHNOLOGY 09

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures - BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

MODULE III NONVOLATILE MEMORIES 09

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS, PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture - Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

MODULE IV MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 09

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

MODULE V RELIABILITY AND RADIATION EFFECTS 09

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

L: 45 - Total Hours:45

REFERENCES

1. Ashok K.Sharma, "Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3. Betty Prince, “Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

OUTCOMES:

On completion of the course the students will be able to

- Discuss the advancements in the SRAM and DRAM based memory technologies
- Analyze and interpret the design parameters used to design memory cells
- Describe the advancements in non-volatile memory design techniques
- Use fault modeling techniques to test memories
- Select appropriate technique to test memory devices
- To use suitable memory devices based on the requirements

ECCY058 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- Analysis of high speed circuits with signal behavior modeling
- Signaling and coding strategies to improve signal integrity in high-speed serial link.
- Analysis procedures for signal measurements.
- clock distributions and clock oscillators

MODULE I SIGNAL PROPAGATION ON TRANSMISSION LINES 07

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters.

MODULE II PRINTED CIRCUIT BOARDS 07

PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmissionline section, reflection coefficient, skin-effect, dispersion.

MODULE III MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS TALK 09

Multi-conductor transmission-lines, coupling physics, per MODULE length parameters, Near and far-end cross-talk, minimizing cross-talk (stipline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

MODULE IV NON-IDEAL EFFECTS 07

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tan d, routing parasitic, Common-mode current, differential-mode current, Connectors.

MODULE V POWER CONSIDERATIONS AND SYSTEM DESIGN 09

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package

types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

MODULE VI CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 6

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter

L: 45 - Total Hours:45

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin, Signal Integrity – Simplified, Prentice Hall PTR, 2003.

OUTCOMES:

On completion of the course the students will be able to

- Describe the signal behavior on high speed circuits such as cross talk in transmission lines
- Analyze the fundamentals of high speed signal propagation in circuits and cables.
- Summarize power consideration and timing analysis and other losses in system design
- Apply the measurement techniques in clock oscillators
- Determine where signal integrity issues
- Solve problems of poor digital signal integrity.

ECCY059 SOC DESIGN AND VERIFICATION

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is to

- Understand the System on Chip with its need, evolution, challenges, goals, superiority over system on board & stacked ICs in package.
- Analyze how the SoCs are designed in industrial environment using different design methodologies
- Analyze the on chip components interconnected in a SoC.
- Analyze and solve problems in traditional bus based communication architecture using network on chip.

MODULE I INTRODUCTION TO LOGIC GATES & COMBINATIONAL LOGIC NETWORKS 09

Introduction to logic gates & combinational logic networks, Combinational Logic Functions, Combinational Network Delay. Logic and interconnect Design. Power Optimization.

MODULE II SYSTEM ON CHIP DESIGN PROCESS 09

A canonical SoC Design, SoC Design flow waterfall vs spiral, topdown vs Bottomup. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure, Logic design issues Verification strategy, Onchip buses and interfaces, Low Power, Manufacturing test strategies.

MODULE III MACRO DESIGN PROCESS 09

Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design, System Integration with reusable macros.

MODULE IV SOC VERIFICATION 09

Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM.

MODULE V DESIGN OF COMMUNICATION ARCHITECTURES FOR SOCS 09

On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

L: 45 - Total Hours:45

REFERENCES

1. PrakashRashinkar Peter Paterson and Leena Singh “SoC Verification Methodology and Techniques”, Kluwer Academic Publishers, 2001.
2. Michael Keating, Pierre Bricaud, “Reuse Methodology manual for System on AChip Designs”, Kluwer Academic Publishers, second edition, 2001.
3. William K. Lam, “Design Verification: Simulation and Formal Method based Approaches”, Prentice Hall.
4. Rochit Rajsuman, “System- on -a- Chip Design and Test”, ISBN.
5. A.A. Jerraya, W.Wolf “Multiprocessor Systemsonchips”, M K Publishers.
6. Dirk Jansen “The EDA HandBook”, Kluwer Academic Publishers.

OUTCOMES:

On completion of the course the students will be able to

- Describe CMOS VLSI Technologies along with performance parameters
- Analyze the top-down and bottom-up design flows, timing problems.
- Design and implement data path elements such as ALUs, Multipliers.
- Investigate various power optimization and timing issues related to complex digital systems
- Use techniques for designing MP SoCs and its performance.
- Illustrate the bus architectures of NOCs and routing.

ECCY060 SOFTWARE FOR EMBEDDED SYSTEMS

L	T	P	C
2	0	2	3

OBJECTIVES:

The objective of the course is

- To know the basic conepts of C Programming.
- To Introduce the GNU C Programming Tool Chain in Linux.
- To understand embedded C and Embedded OS
- To introduce the phython language

MODULE I C PROGRAMMING CONCEPTS 09

Programming Style - Declarations and Expressions - Arrays, Qualifiers and Reading Numbers - Decision and Control Statements - Programming Process - More Control Statements - Variable Scope and Functions - C Preprocessor - Advanced Types - Simple Pointers - Debugging and Optimization.

Laboratory Practice

Practice C language programs illustrating the language constructs in the module I using C compiler

MODULE II C PROGRAMMING TOOLCHAIN IN LINUX 09

Introduction to GCC - Debugging with GDB - The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using gprof - Memory Leak Detection with valgrind - Introduction to GNU C Library .

Laboratory Practice

Practice C language programs using GCC compiler in Linux environment

MODULE III EMBEDDED C USING 8051 MICROCONTROLLER 09

Adding Structure to ‘C’ Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts.

Laboratory Practice

Practice Embedded C language programs illustrating the language construct in the module III using C Keil µvision IDE

MODULE IV EMBEDDED OS 09

Creating embedded operating system: Basis of a simple embedded OS, Introduction to sEOS, Using Timer 0 and Timer 1, Portability issue, Alternative system architecture, Important design considerations when using sEOS.

Laboratory Practice

Practice Embedded C language programs illustrating the language construct in the module IV using C Keil µvision IDE

MODULE V PYTHON PROGRAMMING 09

Basics of PYTHON Programming Syntax and Style – Python Objects– Dictionaries – comparison with C programming on Conditionals and Loops – Files – Input and Output – Errors and Exceptions – Functions – Modules – Classes and OOP – Execution Environment.

Laboratory Practice

Practice basic Python language programs illustrating the language construct in the module V using Python interactive shell software

L: 45 - Total Hours: 45

REFERENCES:

1. Stephen Kochan, “Programming in C”, 3rd Edition, Sams Publishing, 2009.
2. Steve Oualline, ‘Practical C Programming 3rd Edition’, O’Reilly Media, Inc, 2006.
3. Michael J Pont, “Embedded C”, Pearson Education, 2007.
4. Mark Lutz, “Learning Python Powerful OOPs”, O’reilly, 2011.

OUTCOMES

At the end of the course students will be able to

- Write, compile and debug programs in C language.
- compile the program in linux operating system
- Develop program using embedded C
- Describe operating system in embedded system
- Program using phython language
- Design projects using embedded C and python language

ECCY061 TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVES:

To impart knowledge on

- Automated and manual techniques for generating tests for faults in digital circuits and systems.
- Generation of test vectors for combinational and sequential circuits
- Fault diagnosis algorithms

MODULE I BASICS OF TESTING AND FAULT MODELING 09

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

MODULE II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 09

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation -Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

MODULE III DESIGN FOR TESTABILITY 09

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design – System level DFT approaches.

MODULE IV SELF TEST AND TEST ALGORITHMS 09

Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design – Testing of Embedded RAMs.

MODULE V FAULT DIAGNOSIS 9

Logic Level Diagnosis - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

L: 45 - Total Hours:45

REFERENCES

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002
4. A.L. Crouch, "Design Test for Digital ICs and Embedded Core Systems", Prentice Hall International, 2002.

OUTCOMES:

After successful completion of the course, the students will be able to

- Detect faults in digital circuit using logicalfault models
- Generate test vectors using stuck at models for combinational circuits
- Design circuit with testability perspective
- Design test vector for sequential circuits
- Describe the architecture of built in self test and fault diagnosis.
- Diagnose faults in digital circuits at system level

ECCY062 VLSI DIGITAL SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To learn a complete DSP system and fundamentals of pipelining and parallel processing on FIR filters
- To study the concepts of retiming, unfolding, transforms and rank order filters.
- To understand different fast convolution algorithms and pipelining/parallel processing techniques for IIR filters
- To study different bit level architectures and their complexities

MODULE I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 09

Introduction to DSP systems, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

MODULE II RETIMING, ALGORITHMIC STRENGTH REDUCTION 09

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd Even merge-sort architecture

MODULE III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 09

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

MODULE IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 09

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers

with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

MODULE V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 09

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

L: 45 - Total Hours:45

REFERENCES

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

OUTCOMES:

After successful completion of the course, the students will be able to

- Describe various algorithms that can be designed and applied on application specific VLSI architecture
- Design fast convolution algorithms and high speed multipliers to improve the efficiency of DSP processors
- Analyze different number representations, arithmetic based binary representations and complexities involved in it for easier numerical computations on processors
- Identify solution for any research queries on DSP processors.
- Develop advanced DSP filters and processors.
- Develop optimized DSP designs by employing the advantages of VLSI concepts.

ECCY063 WSN ARCHITECTURE AND PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES:

The objective of the course is

- To understand the concepts of sensor networks.
- To understand the programming models of sensor node.
- To learn various algorithms in WSN
- To identify the operating system and processor used in particular sensor node.
- To do case study on WSN applications in surveillance and monitoring.

MODULE I INTRODUCTION TO WSN 09

Introduction to WSN-Challenges for WSNs - Characteristic requirements - Required mechanisms - Single-node architecture -Hardware components-Energy consumption of sensor nodes-Operating systems and execution environments

MODULE II NETWORK ARCHITECTURE 09

Sensor network scenarios- Optimization goals and figures of merit- Design principles for WSNs, Service interfaces of WSNs- Gateway concepts

MODULE III SENSOR NETWORK IMPLEMENTATION 09

Sensor Programming- Introduction to TinyOS Programming and fundamentals of Programming sensors using nesC - Algorithms for WSN – Techniques for Protocol Programming.

MODULE IV PROGRAMMING MODELS 09

An Introduction to the Concept of Cooperating Objects and Sensor Networks-System Architectures and Programming Models

MODULE V WSN APPLICATIONS 09

Case Studies- Wireless sensor networks for environmental monitoring, Wireless sensor networks with mobile nodes, Autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.

L: 45 - Total Hours:45

REFERENCES:

1. Holgerkarl, Andreas Willig, “Protocols and architectures for wireless sensor networks”, John Wiley, 2005.
2. Liljana Gavrilovska, SrdjanKrco, Veljko Milutinovic, Ivan Stojmenovic, Roman Trobec, “Application and Multidisciplinary Aspects of Wireless Sensor Networks”, Springer-Verlag, London Limited 2011.
3. Michel Banâtre, Pedro José Marrón, Anibal Ollero, Adam Wolisz, ”Cooperating Embedded Systems and Wireless Sensor Networks “, John Wiley & Sons, Inc .2008.
4. SeetharamanIyengar, Nandhan, “Fundamentals of Sensor Network Programming Applications and Technology”, John Wiley & Sons,Inc. 2008.

OUTCOMES

At the end of the course students will be able to

- Identify and relate the concepts and components of sensor architecture.
- To understand the programming models of sensor node.
- Choose various algorithms in WSN based on requirement
- Identify the operating system and processor used in particular sensor node.
- Understand usage of WSN in various applications like surveillance and monitoring.
- Implement the techniques for WSN programming

ECCY064 DSP SYSTEM DESIGN

L	T	P	C
2	0	0	2

OBJECTIVES:

The objective of the course is to

- State the basic of DSP processors and its types.
- Infer the architecture and peripherals of DSP processors
- Develop the coding skill for code composer studio and matlab tools
- Design DSP based system with advanced technologies.

MODULE I INTRODUCTION OF DSP PROCESSORS 07

Need for Special Digital Signal Processors, Processor trends: Von Newmann versus Harvard architecture, Architectures of superscalar, fixed and floating point processors, New Digital Signal Processing hardware trends, Selection of processors.

MODULE II DSP PROCESSOR ARCHITECTURE 07

Introduction to a popular DSP from Texas Instruments (TMS330C6000 Series), CPU Architecture, CPU Data Paths and Control, Internal Data / Program Memory. On chip peripherals: Timers - Multi channel buffered serial ports - Extended Direct Memory Access, Interrupts, Pipelining.

MODULE III DSK AND CODE COMPOSER STUDIO 08

Design aspects: Introduction to the C6713 DSK- Code Composer Studio IDE - Matlab and basic skills, FIR filter design techniques and tools, IIR filter design techniques and tools, Sampling, quantization and working with the AIC23 codec, Writing efficient code: optimizing compiler - effect of data types and memory map. TMS320C6713 Assembly language Programming: Instructions Set and Addressing Modes – Linear Assembly.

MODULE IV ADVANCED DSP PROCESSOR 08

Present trends: Current trend in Digital Signal Processors: DSP Controllers – Architecture of TMS320C28XX series DSP and its applications. Architecture trends of other Texas Instruments DSP processors, Analog Devices DS processors: Introduction to Sharc / Tiger Sharc / Blackfin series, Other major vendors in the DSP market and the latest trends.

L: 30 - Total Hours:30

REFERENCES

1. On-line TI materials for the TI C6713 DSK board: http://www.ti.com
2. Naim Dahnoun Digital Signal Processing Implementation using the TMS320C6000
3. DSP Platform, 1st Edition
4. R. Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, John Wiley and Sons, Inc., New York, 2004
5. Sen M. Kuo and Woon-SengGan.Digital Signal Processors: Architectures,
6. Implementations, and Applications,
7. David J Defatta J, Lucas Joseph G & Hodkiss William S ;Digital Signal Processing: A System Design Approach, 1st Edition; John Wiley
8. Andrew Bateman, Warren Yates Digital Signal Processing Design, 1st Edition
9. A.V. Oppenheim and R.W. Schafer, Discrete-Time Signal Processing, Second edition, Prentice- Hall,Upper Saddle River, NJ, 1989
10. John G Proakis, Dimitris G Manolakis Introduction to Digital Signal Processing, 1stEdition.

OUTCOMES:

At the end of the course students will be able to

- Familiarize with the needs of special digital signal processors.
- Get basic knowledge about the DSP processor architectures.
- Learn the design aspects of various DSP processors using different software tools.
- Acquire the current trends in digital signal processors with examples.
- Design trainer kit based on DSP processors and its interfacing techniques.
- Develop the DSP processor based system.

ECCY065 ELECTRONIC DESIGN AUTOMATION TOOLS

L	T	P	C
2	0	0	2

OBJECTIVES:

- To study the concepts of simulation and synthesis of HDLs.
- To understand the concepts of SPICE and circuit simulation using Spice.
- To study the concepts of S-edit and Layout design using S-edit.

MODULE I BASICS OF EDA 07

VLSI Design Automation tools-An overview of the features of practical CAD tools – Modelsim - Leonardo spectrum -Xilinx ISE - Quartus II - VLSI backend tools –IC Station, Cadence and Synopsis.

MODULE II SYNTHESIS OF HDLS 08

Logic synthesis in Verilog – Logic synthesis in VHDL - Finite State Machines synthesis in Verilog – Finite State Machines synthesis in VHDL - Memory synthesis in Verilog – Memory synthesis in VHDL - Performance driven synthesis.

MODULE III SIMULATION OF SPICE 07

Circuit description - DC circuit analysis- Transient analysis - AC circuit analysis - Advanced spice commands and analysis- Models for Semiconductor diodes - Models for Bipolar Junction Transistors - Models for Field Effect Transistors.

MODULE IV SCHEMATIC AND LAYOUT DESIGN 08

Creating a project- Drawing, Selecting and Editing objects -Creating a schematic - Creating a symbol - Importing and Exporting Net lists and Schematics - Simulation and Waveform probing.

L: 30 - TOTAL:30

REFERENCES

1. M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008.
2. M.H.Rashid, Spice for Circuits and Electronics using Pspice, PHI 1995.
3. J.Bhaskar, Verilog Synthesis Primer, Prentice Hall, 1998.
4. J.Bhaskar, A Verilog Primer, Prentice Hall, 2005

OUTCOMES:

On completion of the course the students will be able to

- Explain basic definitions and overview of different tools.
- Understand how to solve simulation, Synthesis of HDLs.
- Select and implement appropriate formulations and algorithms from SPICE.
- Choose an appropriate method to design an S-edit.
- Learn the process of netlist and schematic creation.
- Study the basics of SPICE modeling of all types of transistors.

ECCY066 PROGRAMMING SYSTEM VERILOG

L	T	P	C
2	0	0	2

OBJECTIVES:

The objective of the course is to

- Learn the basics of functional verification languages
- Impart knowledge on the OOPS concepts
- Learn the system verilog language constructs and the functional verification procedures

MODULE I INTRODUCTION TO FUNCTIONAL VERIFICATION LANGUAGES 07

Introduction to System Verilog, System Verilog data types. System Verilog procedures, Interfaces and modports, System Verilog routines.

MODULE II INTRODUCTION TO OBJECT ORIENTED PROGRAMMING 07

Classes and Objects, Inheritance, Composition, Inheritance v/s composition, Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs.

MODULE III SYSTEM VERILOG ASSERTIONS 08

Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing.

MODULE IV COVERAGE DRIVEN VERIFICATION AND FUNCTIONAL COVERAGE IN SV 08

Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis SV and C interfacing: Direct Programming Interface (DPI)

L: 30 - Total Hours:30

REFERENCES

1. Sutherland, Stuart, Davidmann, Simon, Flake “System Verilog for Design” : A Guide to Using System Verilog for Hardware Design and Modeling, Peter2nd ed., 2006

2. Chris Spear “System Verilog for Verification”: A Guide to Learning the Testbench Language Features, , 2006
3. Mintz, Mike, Ekendahl, Robert “Hardware Verification with System Verilog”: An Object-Oriented Framework 2007
4. Bergeron, Janick “Writing Testbenches using System Verilog” 2006
5. Meyyappan Ramanathan “A Practical Guide for System Verilog Assertions”

OUTCOMES:

On completion of the course the student will be able to

- Describe the OOPS concepts
- Describe system verilog syntax and language construct
- Write basic system Verilog constructs to verify digital systems
- Develop assertion constructs to verify digital systems
- Use EDA tools for formal verification
- Write system verilogconstructs for convergence driven verification procedures

ECCY067 SENSORS LAB

L	T	P	C
0	0	2	1

OBJECTIVES:

The objective of the course is to

- Introduce different types of sensors
- Learn how to condition the sensor signal
- Study the operations of the sensors

LIST OF EXPERIMENTS

1. To study characteristics of photosensor and its applications.
2. To study the operation and measurement of thermocouple sensors and to estimate their response times.
3. To study the operation of piezoelectric sensors and its applications.
4. To study the operation of sound sensors and its applications.
5. To study the operation of force sensitivity sensors and analyze the parameters.

Labs incorporate implementation concerns involving interference, isolation, linearity, amplification, and grounding.

OUTCOMES:

At the end of the course students will be able to

- Design and build a temperature control system using analog hardware.
- Measure several sensors and choose one appropriate for the system they are designing and building.
- Measure the sensor output and do the appropriate conversions.
- Identify the sensor for specific application
- Analyze the behavior of the sensors
- Develop the embedded system based application

ECCY068	SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION	L	T	P	C
		1	0	0	1

OBJECTIVES:

The objective of the course is to

- Learn the fundamentals of scripting languages to operate the EDA tools
- Study the basic syntax constructs of PERL scripts

MODULE I OVERVIEW OF SCRIPTING LANGUAGES 05

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

MODULE II PERL 10

PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.

L: 15 - Total Hours:15

REFERENCES

1. Randal L, Schwartz Tom Phoenix, “Learning PERL”, Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly Publications, 3rd Edn., 2000
3. Tom Christiansen, Nathan Torkington, “PERL Cookbook”, Oreilly Publications, 3rd Edn,2000

OUTCOMES:

On completion of the course the students will be able to

- Describe the fundamentals of scripting languages
- Write basic scripts to operate EDA tools
- Apply scripting language like PERL to improve EDA tool flow
- Create scripts to synthesize Digital circuits using CAD tools

EIC6212	INDUSTRIAL AUTOMATION USING PLC, DCS ANDSCADA	L	T	P	C
		3	0	2	4

OBJECTIVES:

- To introduce emerging technological options and platforms for industrial automation
- To explain the architecture of PLC, DCS AND SCADA
- To explore application development for industrial automation
- To provide the appropriate automation solutions and recommendations according to the applications.

MODULE I PROGRAMMABLE LOGIC CONTROLLER: HARDWARE AND BASICOPERATIONS 09

Hard relay logic, Evolution of Programmable logic controller (PLC), Hardware Components of PLC: Input / Output modules, power supplies, isolators, CPU, memory and programming devices. Generic Control system Architecture and IO Assignments, General PLC programming procedures, Developing fundamental ladder logic programs (as per IEC61131) for Boolean operations, PLC basic functions : Register basics, timer functions, counter functions.

MODULE II PROGRAMMABLE LOGIC CONTROLLERS: ADVANCED OPERATIONS, INSTALLATIONS AND TROUBLESHOOTING 09

Developing program control instructions, data manipulation instructions, math instructions, sequencer and shift register instructions, Functional block diagram, Analog control using PLC (PID control configuration, PLC installations and troubleshooting

MODULE III DISTRIBUTED CONTROL SYSTEM 07

Introduction to Distributed control system, DCS architectures, Comparison, Local Control Unit, Process interfacing issues, Operator interfaces - Low level and high level operator interfaces - Operator displays - Engineering interfaces - Low level and high level engineering interfaces, Latest trends and developments.

MODULE IV DATA ACQUISITION SYSTEMS 07

Computers in Process control – Data Loggers – Data acquisition systems (DAS) – Alarms – Direct Digital Control (DDC) - Characteristics of digital data – Controller software – Computer Process interface for Data Acquisition and control –

Supervisory Digital Control (SCADA) -introduction and brief history of SCADA – SCADA Hardware and software.

MODULE V NETWORKING **07**

Signal Conditioners and Its interfaces

LABORATORY: **21**

1. Development of Ladder program for simple on-off applications.
2. Development of Ladder program for Timing and counting applications.
3. Automatic control of level using PLC.
4. Automatic control of temperature using PLC.
5. Control of pressure loop using PLC.
6. Configuring Screens and Graphics (DCS).
7. Programming of HMI interfacing with PLC.
8. Tag Assignments to Field Devices in DCS.
9. DCS based PID control for level loop.
10. Communicate PLC with SCADA.

L: 39, P:21 - Total Hours:60

REFERENCES:

1. W. Bolton, "PLC", Elsevier Newnes 4 John W. Webb Ronald & Areis "PLC"
2. Clarke, G., Reynders, D. and Wright, E., "Practical Modern SCADA Protocols: DNP3, 60870.5 and Related Systems", Newnes, 1st Edition, 2004.
3. Petrezeulla," Programmable Controllers", Mc-Graw Hill, 1989.
4. Michael P.Lucas, "Distributed Control System", Van Nastrand Reinhold Company, New York, 1986.

OUTCOMES:

At the end of the course the student will be able to

- Articulate the main concepts, key technologies, strengths, and limitations of industrial automation
- Identify the architecture and infrastructure of PLC.
- Explain the core issues of PLC, DCS AND SCADA
- Choose the appropriate technologies, algorithms, and approaches for the related issues.
- Identify problems, and explain, analyze, and evaluate various automation solutions
- Attempt to generate new ideas and innovations in industrial automation.

MACY081 SIGNAL PROCESSING TECHNIQUES

L	T	P	C
3	1	0	4

OBJECTIVES:

- To impart knowledge on various mathematical transforms for signal processing applications.

MODULE I LAPLACE TRANSFORMATION FOR CONTINUOUS TIME SIGNALS 06+03

Analog and digital signals - Periodic and aperiodic signals – Spectrum estimation for bandwidth requirement – Laplace Transform – Spectrum estimation – Frequency filtering for spectrum modification – Inverse Laplace Transform – Modified spectrum to get filtered signal.

MODULE II Z -TRANSFORM FOR DISCRETE TIME SIGNALS 12+03

Sampling of continuous time signals for discrete time signals – Nyquist sampling rate - Need for discrete signals – Quantization for digital signal – Z-Transform – Spectrum estimation of discrete signals – Digital filters for spectrum modification – Inverse Z-Transform – Modified spectrum to get filtered signal – Impulse response of digital systems - Bilinear Transform for analog to digital conversion.

MODULE III DISCRETE FOURIER TRANSFORM FOR DISCRETE TIME SIGNALS 09+03

Discrete Fourier Transform – Comparison with Z-Transform – Discrete signals for spectrum estimation – Digital filters for spectrum modification – Inverse Discrete Fourier Transform to get filtered signals – Fast Fourier Transform with decimation in either time or frequency

MODULE IV DISCRETE COSINE TRANSFORM FOR DISCRETE TIME SIGNALS 09+03

One dimensional and two dimensional discrete Cosine transforms – comparison with discrete Fourier transform – image processing applications like filtering & compression – two dimensional transform implementation using successive one dimensional transform – application in JPEG standards – zig zag scanning of transform coefficients – inverse discrete Cosine transform – expansion of compressed images – calculation of compression parameters of CF,RMSE,PSNR &CQ.

MODULE V DISCRETE WAVELET TRANSFORM FOR DISCRETE TIME SIGNALS 09+03

Wavelet – Haar wavelet – one dimensional forward discrete wavelet transform – comparison with discrete Cosine transform - two dimensional transform implementation using successive one dimensional transform – Image processing applications like filtering & compression - application in JPEG 2000 standards – zig zag scanning of transform coefficients – inverse discrete wavelet transform – expansion of compressed images – calculation of compression parameters of CF,RMSE,PSNR &CQ.

L – 45; T – 15; - Total Hours– 60

REFERENCES:

1. Joel L.Schiff – The Laplace Transform: Theory and Applications – Springer – 1999.
2. Alexander D. Poularikas - The Transforms and Applications Handbook – Chapter 6 on Z- Transforms - Boca Raton : CRC Press LLC - 2000.
3. D.Sundararajan – The Discrete Fourier Transform: Theory, Algorithm and Applications – World Scientific Publishers – 2001.
4. K.Rao and P.Yip – Discrete Cosine Transform – Elsevier – 1990.
5. D.Sundararajan – Discrete Wavelet Transform: A Signal Processing Approach – Wiley – 2015.

OUTCOMES:

On completion of the course, the student will be able to apply

- Laplace transform for analog signal analysis.
- Z Transform for discrete signal analysis.
- Discrete Fourier Transform for discrete signal analysis.
- Discrete Cosine Transform for discrete signal analysis.
- Discrete Wavelet Transform for discrete signal analysis.
- Inverse Discrete Wavelet Transform for discrete signal analysis

GENERAL ELECTIVES

GECY101	PROJECT MANAGEMENT	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objectives of the course would be to make the students

- Learn to e valuate and choose an optimal project and build a project profile.
- Attain knowledge on risk identification and risk analysis
- Gain insight into a project plan and components
- Familiar with various gamut of technical analysis for effective project implementation
- Learn to apply project management techniques to manage resources.

MODULE I INTRODUCTION & PROJECT INITIATION 09

Introduction to project and project management - projects in contemporary organization – The project life cycle - project initiation - project evaluation methods & techniques - project selection criteria - project profile.

MODULE II RISK ANALYSIS 09

Sources of risk: project specific - competitive - industry specific - market and international risk – perspectives of risk – risk analysis: sensitivity analysis - scenario analysis - breakeven analysis - simulation analysis - decision tree analysis – managing/mitigating risk – project selection under risk.

MODULE III PROJECT PLANNING & IMPLEMENTATION 09

Project planning – importance – functions - areas of planning - project objectives and policies - steps in planning process - WBS – capital requirements - budgeting and cost estimation - feasibility analysis - creation of project plan – project implementation: pre-requisites - forms of project organization

MODULE IV TECHNICAL ANALYSIS 09

Technical analysis for manufacturing/construction/infrastructure projects – process/technology - materials and inputs - product mix - plant capacity – plant location and site selection – plant layout - machinery and equipment – structures and civil works – schedule of project implementation – technical analysis for software projects.

MODULE V PROJECT MANAGEMENT TECHNIQUES 09

Project scheduling - network construction – estimation of project completion time – identification of critical path - PERT & CPM – crashing of project network - complexity of project scheduling with limited resources - resource allocation - resource leveling – resource smoothing – overview of project management software.

Total Hours: 45

REFERENCES:

1. Projects: Planning, Analysis, Financing, Implementation and Review, Prasanna Chandra, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2004.
2. Project Management and Control, Narendra Singh, Himalaya Publishing, New Delhi, 2015.
3. A Management Guide to PERT/CPM, Jerome, D. Weist and Ferdinand K. Levy, Prentice Hall of India, New Delhi, 1994.

OUTCOMES:

On successfully completing this course, the student will be able to:

- Evaluate & select a project as well as develop a project profile.
- Identify various risks associated with the project and manage it effectively.
- Prepare a detailed project plan addressing its components.
- Perform technical analysis for effective project implementation
- Apply project management techniques for maximizing resource utilization.

GECY102 SOCIETY, TECHNOLGY & SUSTAINABILITY

L	T	P	C
3	0	0	3

OBJECTIVES:

- To aware of new technologies through advances in Science and Engineering.
- To make them realise the profound impact on society.
- To understand the ethical issues raised by technological changes and its effect on society.
- To introduce students a broad range of perspectives on the adoption and use of technologies.
- To make them realize the need of sustainability in the context of emerging technologies.

MODULE I TECHNOLOGY AND ITS IMPACTS 09

Origin and evolution of technologies – Nature of technology- Innovation – Historical Perspective of technology – Sources of technological change - Co-evolution of technology and economy – Scientific knowledge and technological advance – Science and Engineering aspects of Technology – Impact on the Society – Social and Ethical Issues associated with technological change – Social and environmental consequences - Impact of technological change on human life – Technology and responsibility – Technology and social justice.

MODULE II TECHNOLOGY AND ITS ADVANCEMENT 09

Sociological aspects of technology – Ethics and technology – Technology and responsibility – International Economics, Globalisation and Human Rights – Sustainability and Technology – Population and environment - Technology, Energy and Environment – Organisations and technological change.

MODULE III SOCIETY AND TECHNOLOGY 09

Impact of technologies on contemporary society – Role of society in fostering the development of technology – Response to the adaption and use of technology – Impact of technology on developer and consumers – Technological change and globalisation.

MODULE IV IMPACT OF A SPECIFIC TECHNOLOGY ON HUMAN WELFARE 09

Impact of the following technologies on Human life – Medical and Biomedical – Genetics Technology – Electronics and Communications – Electronic media

Technology – Information Systems Technology – Nanotechnology – Space Technology and Energy Technology.

MODULE V THE IMPORTANCE OF SUSTAINABILITY 09

Sustainability – A brief history – Concepts and contexts for sustainability – Ecological imbalance and biodiversity loss – Climate change – Population explosion. Industrial ecology – systems approach to sustainability – Green engineering and technology- sustainable design- sustainable manufacturing- Green consumer movements – Environmental ethics – Sustainability of the planet Earth – Future planning for sustainability.

Total Hours: 45

REFERENCES:

1. Volti Rudi, “Society and Technology Change”, 6th Edition, Worth publishers Inc, USA, 2009.
2. Arthur W.A, “The nature of Technology: What it is and how it evolves”, Free Press, NY, USA, 2009.
3. Winston M and Edelbach R, “Society, Ethics and Technology”, 3rd Edition, San Francisco, USA, 2005.
4. Martin A.A Abraham, “Sustainability Science and Engineering: Defining Principles”, Elsevier Inc, USA, 2006.
5. R.V.G.Menon, “Technology and Society”, Pearson Education, India, 2011.

OUTCOMES:

At the end of this course, the students will be able to

- Understand the benefits of modern technology for the well-being of human life.
- Connect sustainability concepts and technology to the real world challenges.
- Find pathway for sustainable society.

GECY103 ARTIFICIAL INTELLIGENCE

L	T	P	C
3	0	0	3

OBJECTIVES:

- Expose the history and foundations of artificial intelligence.
- Showcase the complexity of working on real time problems underlying the need for intelligent approaches.
- Illustrate how heuristic approaches provide a good solution mechanism.
- Provide the mechanisms for simple knowledge representation and reasoning.
- Highlight the complexity in working with uncertain knowledge.
- Discuss the current and future applications of artificial intelligence.

MODULE I HISTORY AND FOUNDATIONS 08

History – Scope – Influence from life – Impact of computing domains - Agents in environments - Knowledge representation – Dimensions of Complexity – Sample application domains – Agent structure.

MODULE II SEARCH 10

Problem solving as search – State spaces – Uninformed Search – Heuristic search – Advanced search – Constraint satisfaction - Applications.

MODULE III KNOWLEDGE REPRESENTATION AND REASONING 10

Foundations of knowledge representation and reasoning, representing and reasoning about objects, relations, events, actions, time, and space predicate logic, situation calculus, description logics, reasoning with defaults, reasoning about knowledge, sample applications.

MODULE IV REPRESENTING AND REASONING WITH UNCERTAIN KNOWLEDGE 08

Probability, connection to logic, independence, Bayes rule, Bayesian networks, probabilistic inference, sample applications.

MODULE V CASE STUDY AND FUTURE APPLICATIONS 09

Design of a game / Solution for problem in student's domain. Natural Language processing, Robotics, Vehicular automation – Scale, Complexity, Behaviour – Controversies.

Total Hours: 45

TEXT BOOK:

1. Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, Prentice Hall, Third Edition, 2010.
2. David Poole, Alan Mackworth, Artificial Intelligence: Foundations of Computational Agents, Cambridge University Press, 2010.
3. Nils J. Nilsson, The Quest for Artificial Intelligence, Cambridge University Press, Online edition, 2013.
4. Keith Frankish, William M. Ramsey (eds) The Cambridge Handbook of Artificial Intelligence, Cambridge University Press, 2014.

OUTCOMES:

Students who complete this course will be able to

- Discuss the history, current applications, future challenges and the controversies in artificial intelligence.
- Apply principle of AI in the design of an agent and model its actions.
- Design a heuristic algorithm for search problems.
- Analyze and represent the fact using logic for a given scenario
- Represent uncertainty using probabilistic models
- Develop a simple game or solution using artificial intelligence techniques.

GECY104 GREEN COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To focus on the necessity of green computing technology.
- To expose to various issues with information technology and sustainability.
- To attain knowledge on the technologies for enabling green cloud computing.
- To elaborate on the energy consumption issues
- To illustrate a Green and Virtual Data Center
- To develop into a Green IT Technologist.

MODULE I INTRODUCTION 08

Trends and Reasons to Go Green - IT Data Center Economic and Ecological Sustainment - The Growing Green Gap: Misdirected Messaging, Opportunities for Action - IT Data Center “Green” Myths and Realities - PCFE Trends, Issues, Drivers, and Related Factors - Green Computing and Your Reputation- Green Computing and Saving Money- Green Computing and the Environment

MODULE II CONSUMPTION ISSUES 10

Minimizing power usage – Cooling - Electric Power and Cooling Challenges - Electrical – Power -Supply and Demand Distribution - Determining Energy Usage - From Energy Avoidance to Efficiency - Energy Efficiency Incentives, Rebates, and Alternative Energy Sources - PCFE and Environmental Health and Safety Standards- Energy-exposed instruction sets- Power management in power-aware real-time systems.

MODULE III NEXT-GENERATION VIRTUAL DATA CENTERS 09

Data Center Virtualization - Virtualization beyond Consolidation - Enabling Transparency - Components of a Virtual Data Center - Datacenter Design and Redesign - Greening the Information Systems - Staying Green- Building a Green Device Portfolio- Green Servers and Data Centers- Saving Energy

MODULE IV TECHNOLOGIES FOR ENABLING GREEN AND VIRTUAL DATA CENTERS 08

Highly Effective Data Center Facilities and Habitats for Technology - Data Center Electrical Power and Energy Management - HVAC, Smoke and Fire Suppression

- Data Center Location - Virtual Data Centers Today and Tomorrow - Cloud Computing, Out-Sourced, and Managed Services.

MODULE V SERVERS AND FUTURE TRENDS OF GREEN COMPUTING 10

Server Issues and Challenges - Fundamentals of Physical Servers - Types, Categories, and Tiers of Servers - Clusters and Grids - Implementing a Green and Virtual Data Center - PCFE and Green Areas of Opportunity- 12 Green Computer Companies- What's in Green computer science-Green off the Grid aimed for data center energy evolution-Green Grid Consortium- Green Applications- Green Computing Making Great Impact On Research

Total Hours: 45

REFERENCES:

1. Bud E. Smith,"Green Computing Tools and Techniques for Saving Energy, Money, and Resources", Taylor & Francis Group, CRC Press, ISBN-13: 978-1-4665-0340-3, 2014.
2. Jason Harris, "Green Computing and Green IT Best Practices, On Regulations and Industry Initiatives, Virtualization and power management, materials recycling and Tele commuting, Emereo Publishing .ISBN-13: 978-1-9215-2344-1,2014.
3. Ishfaq Ahmed & Sanjay Ranka, "Handbook of Energy Aware and Green Computing", CRC Press, ISBN: 978-1-4665-0116-4, 2013.
4. Kawahara, Takayuki, Mizuno, "Green Computing with Emerging Memory", Springer Publications, ISBN:978-1-4614-0811-6, 2012
5. Greg Schulz, "The Green and Virtual Data Center", CRC Press, ISBN-13:978-1-4200-8666-9, 2009.
6. Marty Poniatowski, "Foundation of Green IT: Consolidation, Virtualization, Efficiency, and ROI in the Data Center", Printice Hall, ISBN: 9780-1-3704-375-0, 2009.

OUTCOMES:

Students who complete this course will be able to

- Demonstrate issues relating to a range of available technologies, systems and practices to support green computing.
- Select appropriate technologies that are aimed to reduce energy consumption.
- Address design issues needed to achieve an organizations' green

computing objectives.

- Analyze the functionality of Data Centers.
- Critically evaluate technologies and the environmental impact of computing resources for a given scenario.
- Compare the impact of Green Computing with other computing techniques.

GECY105 GAMING DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To master event-based programming
- To learn resource management as it relates to rendering time, including level-of-detail and culling.
- To become familiar with the various components in a game or game engine.
- To explore leading open source game engine components.
- To become familiar of game physics.
- To be compatible with game animation.

MODULE I INTRODUCTION 09

Magic Words – What Skills Does a Game Designer Need? – The Most Important Skill -The Five Kinds of Listening-The Secret of the Gifted.

MODULE II THE DESIGNER CREATES AN EXPERIENCE 09

The Game Is Not the Experience -Is This Unique to Games? -Three Practical Approaches to Chasing Rainbows -Introspection: Powers, Perils, and Practice -Dissect Your Feelings -Defeating Heisenberg -Essential Experience.

MODULE III THE EXPERIENCE IN THE PLAYER MIND AND GAME MECHANICS 08

Modeling – Focus -Empathy – Imagination – Motivation – Space – Objects, Attributes, and States – Actions – Rules.

MODULE IV GAMES THROUGH AN INTERFACE 09

Breaking it Down – The Loop of Interaction – Channels of Information – Other Interface.

MODULE V BALANCED GAME MECHANICS 10

Balance – The Twelve Most Common Types of Game Balance – Game Balancing Methodologies - Balancing Game Economies.

Total Hours: 45

REFERENCES:

1. Jesse Schell, "The Art of Game Design: A Book of Lenses", 2nd Edition

ISBN-10: 1466598646, 2014.

2. Ashok Kumar, Jim Etheredge, Aaron Boudreaux, “Algorithmic and Architectural Gaming Design: Implementation and Development", 1st edition, Idea Group, U.S ISBN-10: 1466616342, 2012.
3. Katie Salen Tekinba, Melissa Gresalfi, Kylie Peppler, Rafi Santo, "Gaming the System - Designing with Gamestar Mechanic" MIT Press , ISBN-10: 026202781X, 2014.
4. James M. Van Verth, Lars M. Bishop "Essential Mathematics for Games and Interactive Applications", Third Edition, A K Peters / CRC Press, ISBN-10: 1482250926, 2015.

OUTCOMES:

Students who complete this course will be able to

- Realize the basic history and genres of games
- Demonstrate an understanding of the overall game design process
- Explain the design tradeoffs inherent in game design
- Design and implement basic levels, models, and scripts for games
- Describe the mathematics and algorithms needed for game programming
- Design and implement a complete three-dimensional video game

GECY106 SOCIAL COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To create original social applications, critically applying appropriate theories and effective practices in a reflective and creative manner.
- To critically analyze social software in terms of its technical, social, legal, ethical, and functional features or affordances.
- To encourage the development of effective communities through the design, use, and management of social software.
- To give students with a base of knowledge and advances for them to critically examine existing social computing services.
- To plan and execute a small-scale research project in social computing in a systematic fashion.
- To become familiar with the concept of computational thinking.

MODULE I BASIC CONCEPTS 09

Networks and Relations: Relations and Attributes, Analysis of Network Data, Interpretation of network data -New Social Learning – Four Changes that Shift Work - Development of Social Network Analysis: Sociometric analysis and graph theory, Interpersonal Configurations and Cliques – Analysing Relational Data.

MODULE II SOCIAL LINK 09

Individual Actors, Social Exchange Theory, Social Forces, Graph Structure, Agent Optimization Strategies in Networks – Hierarchy of Social Link Motivation- Social Context.

MODULE III SOCIAL MEDIA 08

Trends in Computing – Motivations for Social Computing – Social Media: Social relationships, Mobility and Social context – Human Computation – Computational Models- Business use of social Media.

MODULE IV SOCIAL INFORMATION FILTERING 09

Mobile Location Sharing – Location based social media analysis – Social Sharing and Social Filtering – Automated recommender Systems – Traditional and Social Recommender Systems.

MODULE V SOCIAL NETWORK STRATEGY 10

Application of Topic Models – Opinions and Sentiments – Recommendation Systems – Language Dynamics and influence in online communities – Psychometric analysis – Case Study: Social Network Strategies for surviving the zombie apocalypse.

Total Hours: 45

REFERENCES:

1. Tony Bingham, Marcia Conner, “The New Social Learning, Connect. Collaborate. Work”, 2nd Edition, ATD Press, ISBN-10:1-56286-996-5, 2015.
2. Nick Crossley, Elisa Bellotti, Gemma Edwards, Martin G Everett, Johan Koskinen, Mark Tranmer, “Social Network Analysis for Ego-Nets”, SAGE Publication, 2015.
3. Zafarani, Abbasi and Liu, Social Media Mining: An Introduction, Cambridge University Press, 2014.
4. Christina Prell, “Social Network Analysis: History, Theory and Methodology”, 1st Edition, SAGE Publications Ltd, 2012.
5. John Scott, “Social Network Analysis”, Third Edition, SAGE Publication, 2013.
6. Jennifer Golbeck, “Analyzing the Social Web”, Elsevier Publication, 2013.
7. Huan Liu, John Salerno, Michael J. Young, “Social computing and Behavioral Modeling”, Springer Publication, 2009.

OUTCOMES:

Students who complete this course will be able to

- Realize the range of social computing applications and concepts.
- Analyze data left after in social media.
- Recognize and apply the concepts of computational models underlying social computing.
- Take out simple forms of social diagnostics, involving network and language models, applying existing analytic tools on social information.
- Evaluate emerging social computing applications, concepts, and techniques in terms of key principles.
- Design and prototype new social computing systems.

GECY107 SOFT COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

The aim of the course is to

- Enumerate the strengths and weakness of soft computing
- Illustrate soft computing methods with other logic driven and statistical method driven approaches
- Focus on the basics of neural networks, fuzzy systems, and evolutionary computing
- Emphasize the role of euro-fuzzy and hybrid modeling methods
- Trace the basis and need for evolutionary computing and relate it with other soft computing approaches

MODULE I SOFT COMPUTING - BASICS 06

Soft computing – Hard Computing – Artificial Intelligence as the basis of soft computing – Relation with logic driven and statistical method driven approaches- Expert systems – Types of problems: Classification, Functional approximation, Optimizations – Modeling the problem – Machine Learning – Hazards of Soft Computing – Current and future areas of research

MODULE II ARTIFICIAL NEURAL NETWORK 12

Artificial Neuron – Multilayer perceptron – Supervised learning – Back propagation network –Types of Artificial Neural Network: Supervised Vs Un Supervised Network – Radial basis function Network – Self Organizing Maps – Recurrent Network – Hopfield Neural Network – Adaptive Resonance Theory – Issues in Artificial Neural Network – Applications

MODULE III FUZZY SYSTEMS 09

Fuzzy Logic – Membership functions – Operators – Fuzzy Inference systems – Other sets: Rough sets, Vague Sets – Fuzzy controllers - Applications

MODULE IV NEURO FUZZY SYSTEMS 09

Cooperative Neuro fuzzy systems – Neural network driven fuzzy reasoning – Hybrid Neuro fuzzy systems – Construction of Neuro Fuzzy systems: Structure Identification phase, Parameter learning phase – Applications

MODULE V EVOLUTIONARY COMPUTING 09

Overview of evolutionary computing – Genetic Algorithms and optimization –

Genetic Algorithm operators – Genetic algorithms with Neural/Fuzzy systems – Variants of Genetic Algorithms– Population based incremental learning – Evolutionary strategies and applications

Total Hours: 45

TEXTBOOKS:

1. Samir Roy, “Introduction to Soft Computing: Neuro-Fuzzy and Genetic Algorithms”, Pearson, 2013
2. Anupam Shukla, Ritu Tiwari and Rahul Kala, “Real life applications of Soft Computing”, CRC press, 2010.
3. Fakhreddine O. Karray, “Soft Computing and Intelligent Systems Design: Theory, Tools and Applications”, Pearson, 2009

OUTCOMES:

At the end of the course the students will be able to

- Enumerate the theoretical basis of soft computing
- Explain the fuzzy set theory
- Discuss the neural networks and supervised and unsupervised learning networks
- Demonstrate some applications of computational intelligence
- Apply the most appropriate soft computing algorithm for a given situation

GECY108 EMBEDDED SYSTEM PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the design of embedded computing systems with its hardware and software architectures.
- To describe entire software development lifecycle and examine the various issues involved in developing software for embedded systems.
- To analyze the I/O programming and Embedded C coding techniques
- To equip students with the software development skills necessary for practitioners in the field of embedded systems.

MODULE I INTRODUCTION OF EMBEDDED SYSTEM 09

Embedded computing – characteristics and challenges – embedded system design process – Overview of Processors and hardware units in an embedded system – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Memory testing – Flash Memory.

MODULE II SOFTWARE TECHNOLOGY 09

Software Architectures, Software development Tools, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance.

MODULE III INPUT/OUTPUT PROGRAMMING 09

I/O Instructions, Synchronization, Transfer Rate & Latency, Polled Waiting Loops, Interrupt – Driven I/O, Writing ISR in Assembly and C, Non Maskable and Software Interrupts

MODULE IV DATA REPRESENTATION IN EMBEDDED SYSTEMS 09

Data representation, Twos complement, Fixed point and Floating Point Number Formats, Manipulating Bits in -Memory, I/O Ports, Low level programming in C, Primitive data types, Arrays, Functions, Recursive Functions, Pointers, Structures & Unions, Dynamic Memory Allocation, File handling, Linked lists, Queues, Stacks.

MODULE V EMBEDDED C 09

Embedded Systems programming in C – Binding & Running Embedded C program in Keil IDE – Dissecting the program - Building the hardware. Basic techniques for reading & writing from I/O port pins – switch bounce - LED Interfacing using Embedded C.

Total Hours: 45

REFERENCES:

1. Marilyn Wolf, "Computers as components ", Elsevier, 2012.
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003.
3. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education
4. Michael Bass, "Programming Embedded Systems in C and C++", Oreilly, 2003.

OUTCOMES:

On completion of this course the student will be able to

- Design the software and hardware components in embedded system
- Describe the software technology
- Use interrupt in effective manner
- Use keil IDE for programming
- Program using embedded C for specific microcontroller
- Design the embedded projects

GECY109 PRINCIPLES OF SUSTAINABLE DEVELOPMENT

L	T	P	C
3	0	0	3

OBJECTIVES:

- To impart knowledge in the concepts and dimensions of sustainable development.
- To gain knowledge on the framework for achieving sustainability.

MODULE I CONCEPT OF SUSTAINABLE DEVELOPMENT 09

Environment and Development - Population poverty and Pollution – Global and Local environmental issues – Resource Degradation- Greenhouse gases – Desertification-industrialization – Social insecurity, Globalization and environment. History and emergence of the concept of sustainable development-Objectives of Sustainable Development.

MODULE II COMPONENTS AND DIMENSIONS OF SUSTAINABLE DEVELOPMENT 09

Components of Sustainability – Complexity of growth and equity – Social economic and environmental dimensions of sustainable development – Environment – Biodiversity – Natural – Resources – Ecosystem integrity – Clean air and water – Carrying capacity – Equity, Quality of Life, Prevention, Precaution – Preservation and Public Participation Structural and functional linking of developmental dimensions.

MODULE III FRAMEWORK FOR ACHIEVING SUSTAINABILITY 09

Operational guidelines – interconnected prerequisites for sustainable development Empowerment of Women, children, Youth, Indigenous People, Non-Governmental Organizations Local Authorities, Business and industry – Science and Technology for sustainable development – performance indicators of sustainability and assessment mechanism – Constraints and barriers for sustainable development.

MODULE IV SUSTAINABLE DEVELOPMENT OF SOCIO ECONOMIC SYSTEMS 09

Demographic dynamics of sustainability – Policies for socio-economic development – Strategies for implementing eco-development programmes Sustainable development through trade – Economic growth – Action plan for implementing sustainable development – Urbanization and sustainable Cities – Sustainable Energy and Agriculture – sustainable livelihoods.

MODULE V SUSTAINABLE DEVELOPMENT AND INTERNATIONAL RESPONSE 09

Role of developed countries in the development of developing countries – international summits – Stockholm to Johannesburg – Rio principles – Agenda-Conventions – Agreements – Tokyo Declaration – Doubling statement – Tran boundary issues integrated approach for resources protection and management

Total Hours: 45

REFERENCES:

1. Sayer J. and Campbell, B., The Science of Sustainable Development: Local Livelihoods and the Global environment - Biological conservation restoration & Sustainability, Cambridge university Press, London, 2003.
2. M.K. Ghosh Roy. and Timberlake, Sustainable Development, Ane Books Pvt. Ltd, 2011.
3. Mackenthun K.M., Concepts in Environmental Management, Lewis Publications London, 1999.
4. APJ Abdul Kalam and Srijan Pal Singh, Target 3 Billion: Innovative Solutions Towards Sustainable Development, Penguin India, 2011

OUTCOMES:

At the end of the course the student will be able to

- Describe the concepts of sustainable development
- Define the components and dimensions of sustainable development
- Outline the Frame work for achieving sustainability.
- State the policies and strategies for implementing sustainable development for Socio economic programmes.
- Examine the role of developed countries in sustainable development.

GECY110	QUANTITATIVE TECHNIQUES IN MANAGEMENT	L	T	P	C
		3	0	0	3

OBJECTIVE:

To impart knowledge on

- Concepts of operations research
- Inventory control in production management
- Financial management of projects
- Decision theory and managerial economics

MODULE I OPERATIONS RESEARCH 09

Introduction to Operations research – Linear programming – Graphical and Simplex Methods, Duality and Post-Optimality Analysis – Transportation and Assignment Problems

MODULE II PRODUCTION MANAGEMENT 09

Inventory control, EOQ, Quantity Discounts, Safety Stock – Replacement Theory – PERT and CPM – Simulation Models – Quality Control.

MODULE III FINANCIAL MANAGEMENT 09

Working Capital Management – Compound Interest and Present Value methods – Discounted Cash Flow Techniques – Capital Budgeting.

MODULE IV DECISION THEORY 09

Decision Theory – Decision Rules – Decision making under conditions of certainty, risk and uncertainty – Decision trees – Utility Theory.

MODULE V MANAGERIAL ECONOMICS 09

Cost concepts – Break even Analysis – Pricing techniques – Game Theory applications.

Total Hours: 45

REFERENCES:

1. Vohra, N.D. , Quantitative Techniques in Management, Tata McGraw Hill Co., Ltd, New Delhi, 2009.
2. Seehroeder, R.G., Operations Management, McGraw Hill, USA, 2002.
3. Levin, R.I, Rubin, D.S., and Stinsonm J., Quantitative Approaches to Management, McGraw Hill Book Co., 2008.

4. Frank Harrison, E., The Managerial Decision Making Process, Houghton Miffin Co. Boston, 2005.
5. Hamdy A. Taha, Operations Research- An Introduction, Prentice Hall, 2002.

OUTCOME:

At the end of the course, the students will be able to

- Apply the concepts of operations research for various applications
- Create models for inventory control in production management
- Compute the cash flow for a project
- Choose a project using decision theory based on the risk criterion.
- Apply the concepts of managerial economics in construction management

GECY111 PROGRAMMING USING MATLAB & SIMULINK

L	T	P	C
1	0	2	2

OBJECTIVES:

The aim of this course is to:

- Teach students how to mathematically model engineering systems
- Teach students how to use computer tools to solve the resulting mathematical models. The computer tool used is MATLAB and the focus will be on developing and solving models of problems encountered in engineering fields

MODULE I INTRODUCTION TO MATLAB AND DATA PRESENTATION 10

Introduction to MATLAB-Vectors, Matrices -Vector/Matrix Operations & Manipulation- Functions vs scripts- Making clear and compelling plots-Solving systems of linear equations numerically and symbolically.

Lab Experiments

1. Study of basic matrix operations and manipulations.
2. Numerical and symbolical solution of linear equations.

MODULE II ROOT FINDING AND MATLAB PLOT FUNCTION 10

Linearization and solving non-linear systems of equations- The Newton-Raphson method- Integers and rational numbers in different bases- Least squares regression -Curve fitting-Polynomial fitting and exponential fitting.

Lab Experiments

1. Solution of non linear equations using Newton-Raphson method.
2. Determination of polynomial fit and exponential fit for the given data.

MODULE III LINEAR AND NON-LINEAR DIFFERENTIAL EQUATIONS 13

Numerical integration and solving first order, ordinary differential equations (Euler's method and Runge-Kutta) - Use of ODE function in MATLAB- Converting second order and higher ODEs to systems of first order ODEs- Solving systems of higher order ODEs via Euler's method and Runge-Kutta) - Solving single and systems of non-linear differential equations by linearization-Use of the function ODE in MATLAB to solve differential equations - Plot Function –Saving & Painting Plots.

Lab Experiments

1. Solution of fourth order linear differential equations using
    a. Trapezoidal Rule

b. Euler method

2. Solution of fourth order non-linear differential equations using
    a. Modified Euler method
    b. Runge – Kutta method

MODULE IV INTRODUCTION OF SIMULINK 12

Simulink & its relations to MATLAB – Modeling a Electrical Circuit- Modeling a fourth order differential equations- - Representing a model as a subsystem- Programme specific Simulink demos.

Lab Experiments

1. Solution of fourth order non-linear differential equations using simulink.
2. Programme specific experiment based on simulink.

Total Hours (Including Practicals): 45

REFERENCE:

1. Griffiths D V and Smith I M, “Numerical Methods for Engineers”, Blackwell, 1991.
2. Laurene Fausett, “Applied Numerical Analysis Using MATLAB”, Pearson 2008.
3. Moin P, “Fundamentals of Engineering Numerical Analysis”, Cambridge University Press, 2001.
4. Wilson HB, Turcotte LH, Advanced mathematics and mechanics applications using MATLAB”, CRC Press, 1997
5. Ke Chen, Peter Giblin and Alan Irving, “Mathematical Exploration with MATLAB”, Cambridge University Press, 1999.

OUTCOMES:

At the end of this unit students will be able to:

- Use Matlab as a convenient tool for solving a broad range of practical problems in engineering from simple models to real examples.
- Write programs using first principles without automatic use of built-in ones.
- Write programs for solving linear and nonlinear systems, including those arising from boundary value problems and integral equations, and for root-finding and interpolation, including piecewise approximations.
- Be fluent in exploring Matlab’s capabilities, such as using matrices as the fundamental data-storage unit, array manipulation, control flow, script and function m-files, function handles, graphical output.
- Make use of Maltab visual capabilities for all engineering applications.

- An ability to identify, formulate, and solve engineering problems. This will be accomplished by using MATLAB to simulate the solution to various problems in engineering fields

GECY112 JAVA PROGRAMMING

L	T	P	C
1	0	2	2

OBJECTIVES:

- To learn the fundamentals of Java programming such as data types, variables and arrays.
- To study the syntax and necessity of decision making and iterative statements.
- To create a class and invoke the methods.
- To instigate programming in overloading of methods.
- To emphasize the concept of packages.
- To learn the exception handling routines.

MODULE I INTRODUCTION TO JAVA PROGRAMMING 08

History and Evolution of Java – Overview of Java – Data types, variables and arrays – Operators – Control statements.

MODULE II METHODS AND CLASSES 07

Class fundamentals – Declaring objects – Methods – Constructors – Garbage collection – Overloading methods – Constructor overloading – Access control – Inheritance – Packages - Exception handling.

L: 15, P: 30, Total Hours: 15

REFERENCES:

1. Herbert Schildt, “Java The Complete Reference”, 9th Edition, Oracle Press, 2014, ISBN: 978007180855-2.
2. Nicholas S. Williams, **“**Professional Java for Web Applications: Featuring WebSockets, Spring Framework, JPA Hibernate and Spring Security (WROX)”, John Wiley & Sons, 2014, ISBN: 978111865651-8.
3. E Balagurusamy, “Programming with Java”, 5th Edition, Tata Mcgraw Hill, 2014.
4. Yashavant Kanetka**, “**Let Us Java”, 2nd Edition, BPB Publications, 2012**.**

OUTCOMES:

Students who complete this course will be able to

- Implement basic Java programming.
- Create a class and invoke methods for real world problems.

- Construct simple overloading of methods programs.
- Implement various types of inheritance concepts.
- Describe the access control mechanism.
- Handle exception thrown while implementing programming.

GECY113 PYTHON PROGRAMMING

L	T	P	C
1	0	2	2

OBJECTIVES:

- To learn the list and records of python programming.
- To study the control statements and string functions of python.
- To instigate the fundamental python programming.
- To emphasize GUI in python.
- To integrate python with embedded systems.
- To implement programs in python.

MODULE I INTRODUCTION TO PYTHON PROGRAMMING 08

Installation and environment set up – syntax used in python – variable types – operators – Loops – decision making – string functions - formatted files - GUI basics.

MODULE II EMBEDDED PROGRAMMING USING PYTHON 07

Web interface – system tools – script execution context - Motion-triggered LEDs – Python - Arduino prototyping-storing and plotting Arduino data-Remote home monitoring system.

L: 15, P: 30, Total Hours: 15

REFERENCES:

1. Nick Goddard, “Python Programming”, 2nd edition, ISBN: 1533337772, 2016.
2. Pratik Desai, “Python Programming for Arduino”, 1st edition, Packt publishing, 2015, ISBN: 9781783285938.
3. Mark Lutz, Learning Python: Powerful Object-Oriented Programming, 5th Edition, O'Reilly Media, 2013.
4. Richard H. Barnett, Sarah Cox, Larry O'Cull, “Embedded C Programming and the Atmel AVR”, 2nd edition, 2006.
5. Michael Barr, Anthony Massa, “Programming Embedded Systems”, 2nd Edition, O'Reilly Media, 2006.

OUTCOMES:

Students who complete this course will be able to

- Implement date and time function programming using python.

- Write formatted file programming.
- Construct simple python programs.
- Create web interface using python programming
- Develop embedded system with python programming.
- Build Arduino prototype using python programming.

GECY114 INTELLECTUAL PROPERTY RIGHTS (IPR)

L	T	P	C
1	0	0	1

OBJECTIVES:

- To study about Intellectual property rights and its need
- To explore the patent procedure and related issues

MODULE I INTRODUCTION 07

Introduction and the need for intellectual property right (IPR) – IPR in India – Genesis and Development – IPR in abroad – Important examples of IPR – Copyrights, Trademarks, Patents, Designs, Utility Models, Trade Secrets and Geographical Indications – Industrial Designs

MODULE II PATENT 08

Concept of Patent – Product / Process Patents & Terminology – Duration of Patents – Law and Policy Consideration Elements of Patentability –- Patentable Subject Matter – Procedure for Filing of Patent Application and types of Applications – Procedure for Opposition – Revocation of Patents – Working of Patents- Patent Agent – Qualification and Registration Procedure – Patent databases and information system – Preparation of patent documents – Process for examination of patent application- Patent infringement – Recent developments in patent system

Total Hours: 15

REFERENCES

1. B.L.Wadehra; Law Relating to Patents, Trade Marks, Copyright, Designs & Geographical Indications; Universal law Publishing Pvt. Ltd., India 2000
2. Ajit Parulekar and Sarita D' Souza, Indian Patents Law – Legal & Business Implications; Macmillan India ltd , 2006
3. P. Narayanan; Law of Copyright and Industrial Designs; Eastern law House, Delhi, 2010.
4. E. T. Lokganathan, Intellectual Property Rights (IPRs): TRIPS Agreement & Indian Laws Hardcover, 2012
5. Alka Chawla, P N Bhagwati , Law of Copyright Comparative Perspectives 1st Edition, LexisNexis, 2013
6. V. K. Ahuja, Law Relating to Intellectual Property Rights 2nd Edition, LexisNexis, 2nd Edition, 2013

7. Deborah E. Bouchoux, Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 2015
8. Jatindra Kumar Das, Law of Copyright, PHI Learning, 2015

COURSE OUTCOMES:

Students should be able to

- Identify the various types of intellectual property and their value
- Apply the procedure to file a patent and to deal the related issues
- Search and extract relevant information from various intellectual database