B.S.ABDUR RAHMAN
U N I V E R S I T Y
B.S.ABDUR RAHMAN INSTITUTE OF SCIENCE & TECHNOLOGY
(Estd.u/s 3 of the UGC Act, 1956)
(FORMERLY B.S.ABDUR RAHMAN CRESCENT ENGINEERING COLLEGE)
Seethakathi Estate, G.S.T. Road, Vandalur, Chennai - 600 048.

REGULATIONS (2009), CURRICULUM AND SYLLABUS
FOR
M.Tech. (VLSI & EMBEDDED SYSTEMS)
(FOUR SEMESTERS - FULL TIME)

(updated upto June 2012)

REGULATIONS -2009 FOR
M.TECH / MCA / M. Sc DEGREE PROGRAMMES

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires

i) **"Programme"** means Post Graduate Degree Programme (M.Tech./ MCA / M.Sc.)

ii) **"Course"** means a theory or practical subject that is normally studied in a semester, like Applied Mathematics, Structural Dynamics, Computer Aided Design, etc.

iii) **"University"** means B.S.Abdur Rahman University, Chennai, 600048.

iv) **"Institution"** unless otherwise specifically mentioned as an autonomous or off campus institution means B.S.Abdur Rahman University.

v) **"Academic Council"** means the Academic Council of the University.

vi) **'Dean (Academic Courses)'** means Dean (Academic Courses) of B.S.Abdur Rahman University.

vii) **'Dean (Students)'** means Dean(Students) of B.S.Abdur Rahman University.

viii) **"Controller of Examinations"** means the Controller of Examinations of B.S.Abdur Rahman University who is responsible for conduct of examinations and declaration of results.

2.0 PROGRAMMES OFFERED, MODE OF STUDY AND ADMISSION REQUIREMENTS

2.1 P.G. Programmes Offered

The various P.G. Programmes and their modes of study are as follows:

Degree	Mode of study
M.Tech.	Full Time
M.Tech.	Part Time – Day / Evening
M.C.A.	Full Time
M. Sc.	Full Time

2.2 MODES OF STUDY

2.2.1 Full-time

Candidates admitted under "Full-Time" shall be available in the institution during the complete working hours for curricular, co-curricular and extra-curricular activities assigned to them.

2.2.2 A full time student, who has completed all non-project courses desiring to do the Project work in part-time mode for valid reasons, shall apply to the Head of the Institution through the Head of the Department, if the student satisfies the clause 2.3.5 of this Regulations. Permission may be granted based on merits of the case. Such conversion is not permitted in the middle of a semester.

2.2.3 Part time - Day time

In this mode of study, the candidates are required to attend classes for the courses registered along with full time students.

2.2.4 Part time - Evening

In this mode of study, the candidates are required to attend only evening classes.

2.2.5 A part time student is not permitted to convert to the full time mode of study.

2.3. ADMISSION REQUIREMENTS

2.3.1 Candidates for admission to the first semester of the Master's Degree Programme shall be required to have passed an appropriate degree examination of this University as specified in Table 1 or any other examination of any University or authority accepted by the University as equivalent thereto.

2.3.2 Notwithstanding the qualifying examination the candidate might have passed, he/she shall have a minimum level of proficiency in the appropriate programme/courses as prescribed by the institution from time to time.

2.3.3 Eligibility conditions for admission such as class obtained, number of attempts in qualifying examination and physical fitness will be as prescribed by the Institution from time to time.

2.3.4 All part-time candidates should satisfy other conditions regarding experience, sponsorship etc., which may be prescribed by the institution from time to time.

2.3.5 A candidate eligible for admission to M.Tech. Part Time - Day Time programmeshall have his/her permanent place of work within a distance of 65km from the campus of the institution.

2.3.6 A candidate eligible for admission to M.B.A. Part Time - Evening programme shall have a working experience of 2 years at least at supervisory level. He/ she shall have his/her place of work within a distance of 65 km from the campus of the institution.

3.0 DURATION AND STRUCTURE OF THE P.G. PROGRAMME

3.1. The minimum and maximum period for completion of the P.G. Programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M.Tech. (Full Time)	4	8
M.Tech.(Part Time)	6	12
M.C.A. (Full Time)	6	12
M.Sc. (Full Time)	4	8

3.2 The P.G. programmes will consist of the following components as prescribed in the respective curriculum

i. Core courses

ii. Elective courses

iii. Project work / thesis / dissertation

iv. Laboratory Courses

v. Case studies

vi. Seminars

vii. Practical training

3.3 The curriculum and syllabi of all the P.G. programmes shall be approved by the Academic Council.

3.4 The number of credits to be earned for the successful completion of the programme shall be specified in the curriculum of the respective specialization of the P.G. programme.

3.5 Each academic semester shall normally comprise of 75 to 80 working days spread over sixteen weeks. End-semester examinations will follow immediately after these working days.

ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO P.G. PROGRAMMES

Sl.No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
01.	Civil Engineering	M.Tech. (Structural Engineering)	B.E / B.Tech. (Civil Engineering) / (Structural Engineering)
		M.Tech. (Construction Engineering and Project Management)	B.E. / B.Tech. (Civil Engineering) /(Structural Engineering)
02.	Mechanical Engineering	M.Tech. (CAD - CAM)	B.E. / B.Tech. (Mechanical / Auto /Manufacturing / Production / Industrial/Mechatronics / Metallurgy / Aerospace/Aeronautical / Material Science / Marine Engineering)
		M.Tech. (Manufacturing Engineering)	B.E. / B.Tech. (Mechanical / Auto / Manufacturing / Production / Industrial/Mechatronics / Metallurgy / Aerospace/Aeronautical / Material Science / Marine Engineering)
03.	Polymer Technology	M.Tech. (Polymer Technology)	B. E. / B. Tech. degree Mech./ Production / Polymer Science or Engg or Tech/Rubber Tech/ M.Sc(Polymer Sc./Chemistry Appl. Chemistry)
04.	Electrical and Electronics Engineering	M.Tech. (Power Systems Engg)	B.E/B.Tech (EEE/ECE/E&I/ I&C/ Electronics / Instrumentation)
		M.Tech. (Power Electronics & Drives)	B.E/B.Tech (EEE/ECE/E&I/ I&C/ Electronics/ Instrumentation)
05.	Electronics and Communication Engineering	M.Tech. (Communication Systems)	M.Tech (Power System Engg) B.E / B.Tech (EEE/ ECE / E&I / I&C / Electronics / Instrumentation) B.E./ B.Tech. in ECE / Electronics / EIE
		M.Tech. (VLSI and Embedded Systems)	
06.	ECE Department jointly with Physics Department	M.Tech. (Optoelectronics and Laser Technology)	B.E./B.Tech. (ECE / EEE / Electronics / EIE / ICE) M.Sc (Physics / Materials Science / Electronics / Photonics)
07.	Electronics and Instrumentation Engineering	M.Tech. (Electronics and Instrumentation Engineering)	B.E./B.Tech. (EIE/ICE/Electronics/ECE/EEE)
08.	Computer Science and Engineering	M.Tech. (Computer Science and Engineering)	B.E. /B.Tech. (CSE/IT/ECE/EEE/EIE/ICE/ Electronics / MCA)
		M.Tech. (Software Engineering)	B.E. / B.Tech. (CSE / IT) MCA
09	Information Technology	M.Tech. (Information Technology)	B.E /B.Tech. (IT/CSE/ECE/EEE/EIE/ICE/ Electronics) MCA
10	Computer Applications	M.C.A.	Any degree. Must have studied Mathematics / Statistics /Computer oriented subject.
		M.Tech. (Systems Engineering and Operations Research)	Any degree. Must have studied Mathematics / Statistics /Computer oriented subject.
11	Mathematics	M.Sc. (Actuarial Science)	B.Sc. (Mathematics) of B.Sc. (Applied Science)
12	Chemistry	M.Sc.(Chemistry)	B.Sc (Chemistry) of B.Sc. (Applied Science)

3.6 The curriculum of P.G. programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall lie within the limits specified below:

Programme	Minimum prescribed credit range
M.Tech.	70 to 80
M.C.A	130 to 140
M.Sc	74 to 80

3.7 Credits will be assigned to the courses for all P.G. programmes as given below:

* One credit for one lecture period per week
* One credit for one tutorial period per week
* One credit each for seminar/practical session of two or three periods per week
* One credit for four weeks of practical training

3.8 The number of credits registered by a candidate in non-project semester and project semester should be within the range specified below:

P.G. Programme	Non-project Semester	Project semester
M.Tech. (Full Time)	15 to 23	12 to 20
M.Tech. (Part Time)	6 to 12	12 to 16
M.C.A. (Full Time)	12 to 25	12 to 20
M.Sc. (Full Time)	15 to 25	12 to 20

3.9 The electives from the curriculum are to be chosen with the approval of the Head of the Department.

3.10 A candidate may be permitted by the Head of the Department to choose electives offered from other P.G. Programmes either within a Department or from other Departments up to a maximum of three courses during the period of his/her study, provided the Heads of the Departments offering such courses also agree.

3.11 To help the students to take up special research areas in their project work and to enable the department to introduce courses in latest/emerging areas in the curriculum, "Special Electives" may be offered. A candidate may be

permitted to register for a "Special Elective" up to a maximum of three credits during the period of his/her study, provided the syllabus of this course is recommended by the Head of the Department and approved by the Dean (AC) before the commencement of the semester, in which the special elective course is offered. Subsequently, such course shall be ratified by the Board of Studies and Academic Council.

3.12 The medium of instruction, examination, seminar and project/thesis/ dissertation reports will be English.

3.13 Practical training or industrial attachment, if specified in the curriculum shall be of not less than four weeks duration and shall be organized by the Head of the Department.

3.14 PROJECT WORK/THESIS/DISSERTATION

3.14.1 Project work / Thesis / Dissertation shall be carried out under the supervision of a qualified teacher in the concerned Department.

3.14.2 A candidate may however, in certain cases, be permitted to work on the project in an Industrial/Research Organization, on the recommendation of Head of the Department, with the approval of the Head of the Institution. In such cases, the project work shall be jointly supervised by a supervisor of the Department and an Engineer / Scientist from the organization and the student shall be instructed to meet the supervisor periodically and to attend the review committee meetings for evaluating the progress.

3.14.3 Project work / Thesis / Dissertation (Phase - II in the case of M.Tech.) shall be pursued for a minimum of 16 weeks during the final semester, following the preliminary work carried out in Phase-1 during the previous semester.

3.14.4 The Project Report/Thesis / Dissertation report / Drawings prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the Head of the Institution.

3.14.5 The deadline for submission of final Project Report / Thesis / Dissertation is within 30 calendar days from the last working day of the semester in which Project / Thesis / Dissertation is done.

3.14.6 If a candidate fails to submit the Project Report / Thesis / Dissertation on or before the specified deadline he / she is deemed to have not completed the Project Work / Thesis / dissertation and shall re-register the same in a subsequent semester.

3.14.7 A student who has acquired the minimum number of total credits prescribed in the Curriculum for the award of the Masters Degree will not be permitted to enroll for more courses to improve his/her cumulative grade point average (CGPA).

4.0 FACULTY ADVISER

To help the students in planning their courses of study and for getting general advice on academic programme, the concerned department will assign a certain number of students to a faculty member who will be called the Faculty Adviser.

5.0 CLASS COMMITTEE

5.1 Every class of the P.G. Programme will have a Class Committee, constituted by the Head of the Department as follows:

i. Teachers of all courses of the programme

ii. One senior faculty preferably not offering courses for the class, as chairperson.

iii. One or two students of the class, nominated by the Head of the Department.

iv. Faculty Advisers of the class - Ex-Officio Members

v. Professor in-charge of the P.G. Programme - Ex-Officio Member.

5.2 The Class Committee shall be constituted by the respective head of the department of the students.

5.3 The basic responsibilities of the Class Committee are to review periodically the progress of the classes, to discuss problems concerning curriculum and syllabi and the conduct of the classes. The type of assessment for the course will be decided by the teacher in consultation with the Class Committee and will be announced to the students at the beginning of the semester. Each Class Committee will communicate its recommendations to the Head of the Department and the Head of the Institution. The class committee, **without the student members,** will also be responsible for finalization of the semester results.

5.4 The Class Committee is required to meet at least thrice in a semester, once at the beginning of the semester, another time after the end-semester examination to finalise the grades, and once in between.

6.0 COURSE COMMITTEE

Each common theory course offered to more than one group of students shall have a "Course Committee" comprising all the teachers teaching the common course with one of them nominated as Course coordinator. The nomination of the Course coordinator shall be made by the Head of the Department / Head of the Institution depending upon whether all the teachers

teaching the common course belong to a single department or to several departments. The Course Committee shall meet as often as possible and ensure uniform evaluation of the tests and arrive at a common scheme of evaluation for the tests. Wherever it is feasible, the Course Committee may also prepare a common question paper for the test(s).

7.0 REGISTRATION AND ENROLMENT

7.1 For the first semester every student has to register and enroll for the courses he/she intends to undergo on a specified day notified to the student. The concerned Faculty Adviser will be present and guide the students in the registration/enrolment process.

7.2 For the subsequent semesters registration for the courses will be done by the student during a specified week before the end-semester examination of the previous semester. The curriculum gives details of the core and elective courses, project and seminar to be taken in different semester with the number of credits. The student should consult his/her Faculty Adviser for the choice of courses. The Registration form is filled in and signed by the student and the Faculty Adviser.

7.3 Late registration will be permitted with a prescribed fine up to two weeks from the last date specified for registration.

7.4 From the second semester onwards all students shall pay the prescribed fees and enroll on a specified day at the beginning of a semester.

A student will become eligible for enrolment only if he/she satisfies clause 9 and in addition he/she is not debarred from enrolment by a disciplinary action of the Institution. At the time of enrolment a student can drop a course registered earlier and also substitute it by another course for valid reasons with the consent of the Faculty Adviser. Late enrolment will be permitted on payment of a prescribed fine up to two weeks from the date of commencement of the semester.

7.5 Withdrawal from a course registered is permitted up to one week from the date of the completion of the first assessment test.

7.6 Change of a course within a period of 15 days from the commencement of the course, with the approval of Dean (AC), on the recommendation of the HOD, is permitted.

7.6.1 Courses withdrawn will have to be taken when they are offered next if they belong to the list of core courses.

7.7 SUMMER TERM COURSES

7.7.1 Summer term courses may be offered by a department on the recommendation by the Departmental Consultative Committee and approved by the Head of the Institution. No student should register for more than three courses during a summer term.

7.7.2 Summer term courses will be announced by the Head of the Institution at the end of the even semester before the commencement of the end semester examinations. A student will have to register within the time stipulated in the announcement. A student has to pay the fees as stipulated in the announcement.

7.7.3 Fast-track summer courses of 30 periods for 3 credit courses and 40 periods for 4 credit courses will be offered for students with I grades. They may also opt to redo such courses during regular semesters with slotted time-tables. Students with U grades will have the option either to write semester end arrears exam or to redo the courses during summer / regular semesters with slotted time-table, if they wish to improve their continuous assessment marks also.

The assessment procedure in a summer term course will also be similar to the procedure for a regular semester course.

7.7.4 Withdrawal from a summer term course is not permitted. No substitute examination will be held for the summer term courses.

8.0 TEMPORARY WITHDRAWAL FROM THE PROGRAMME

A student may be permitted by the Head of the Institution to temporarily withdraw from the programme up to a maximum of two semesters for reasons of ill health or other valid grounds. However the total duration for completion of the programme shall not exceed the prescribed number of semesters (vide clause 3.1).

9.0 MINIMUM REQUIREMENTS TO REGISTER FOR PROJECT / THESIS / DISSERTATION

9.1 A candidate is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	Minimum No. of credits to be earned to enrol for project semester
M.Tech. (Full time)	18 (III semester)
M.Tech. (Part-time)	18 (V semester)
M.C.A. (Full time)	45 (VI semester)
M.Sc. (Full-time)	28 (IV semester)

9.2 **M.Tech.:** If the candidate has not earned minimum number of credits specified, he/she has to earn the required credits (at least to the extent of minimum credit specified in clause 9.1) and then register for the project semester.

9.3 **M.C.A.:** If the candidate has not earned the required minimum number of credits specified he/she has to earn the required credits (at least to the extent of minimum credits specified in clause 9.1) and then register for the project work in subsequent semesters.

10.0 DISCIPLINE

10.1 Every candidate is required to observe discipline and decorous behaviour both inside and outside the campus and not to indulge in any activity, which will tend to bring down the prestige of the institution.

10.2 Any act of indiscipline of a candidate reported to the Head of the Institution will be referred to a Discipline and Welfare Committee for taking appropriate action.

10.3 Every candidate should have been certified by the HOD that his / her conduct and discipline have been satisfactory.

11.0 ATTENDANCE

11.1 Attendance rules for all Full Time Programme and Part time - day Time Programmes are given in the following sub-clauses.

11.2 A student **shall earn 100% attendance** in the contact periods of every course, subject to a **a maximum relaxation of 25%** for genuine reasons like on medical grounds , representing the University in approved events etc., to become eligible to appear for the end-semester examination in that course, failing which the student shall be awarded "I" grade in that course. If the course is a core course, the candidate should register for and repeat the course when it is offered next.

12.0 ASSESSMENTS AND EXAMINATIONS

12.1 The following rule shall apply to the full-time and part-time P.G. programmes (M.Tech./ M.C.A. / M.Sc.)

For lecture-based courses, normally a minimum of two assessments will be made during the semester. The assessments may be combination of tests and assignments. The assessment procedure as decided at the Class Committee will be announced to the students right at the beginning of the semester by the teacher and informed to Dean(AC)

12.2 There shall be one **examination** of three hours duration, at the end of the semester, in each lecture based course.

12.3 The evaluation of the Project work will be based on the project report and a Viva-Voce Examination by a team consisting of the supervisor concerned, an Internal Examiner and External Examiner to be appointed by the Controller of Examinations.

12.4 At the end of practical training or industrial attachment, the candidate shall submit a certificate from the organization where he/she has undergone training and also a brief report. The evaluation will be made based on this report and a Viva-Voce Examination, conducted internally by a Departmental Committee constituted by the Head of the Department.

13.0 WEIGHTAGES

13.1 The following shall be the weightages for different courses:

i)	**Lecture based course**		
	Two sessional assessments	-	50%
	End-semester examination	-	50%
ii)	**Laboratory based courses**		
	Laboratory work assessment	-	75%
	End-semester examination	-	25%
iii)	**Project work**		
	Periodic reviews	-	50%
	Evaluation of Project Report by External Examiner	-	20%
	Viva-Voce Examination	-	30%

13.2 The markings for all tests, tutorial assignments (if any), laboratory work and examinations will be on absolute basis. The final percentage of marks is calculated in each course as per weightages given in clause 13.1.

14.0 SUBSTITUTE EXAMINATION

14.1 A student who has missed for genuine reasons any one of the three assessments including end-semester examination of a course may be permitted to write a substitute examination. However, permissions to take up a substitute examination will be given under exceptional circumstances, such as accident or admissions to a hospital due to illness, etc.,

14.2 A student who misses any assessment in a course shall apply in a prescribed form to the Dean(AC) through the Head of the department within a week from the date of missed assessment. However the substitute tests and examination for a course will be conducted within two weeks after the last day of the end-semester examinations.

15.0 COURSEWISE GRADING OF STUDENTS AND LETTER GRADES:

15.1 Based on the semester performance, each student is awarded a final letter grade at the end of the semester in each course. The letter grades and the corresponding grade points are as follows, but grading has to be relative grading

Letter grade	Grade points
S	10
A	9
B	8
C	7
D	6
E	5
U	0
I	-
W	-

Flexible range grading system will be adopted

"W" denotes withdrawal from the course.

"I" denotes inadequate attendance and hence prevention from End Semester examination.

"U" denotes unsuccessful performance in a course.

15.2 A student is considered to have completed a course successfully and earned the credits if he / she secure five grade points or higher. A letter grade U in any course implies unsuccessful performance in that course. A course successfully completed cannot be repeated for any reason.

16.0 METHOD OF AWARDING LETTER GRADE:

16.1 A final meeting of the Class Committee without the student member(s) will be convened within ten days after the last day of the semester end examination. The letter grades to be awarded to the students for different courses will be finalized at the meeting.

16.2 Three copies of the results sheets for each course, containing the final grade and three copies with the absolute marks and the final grade should be submitted by the teacher to the concerned Class Committee Chairman. After finalisation of the grades at the class committee meeting the Chairman will forward two copies of each to the Controller of Examinations and the other copies to the Head of the Department in which course is offered.

17.0 DECLARATION OF RESULTS:

17.1 After finalisation by the Class Committee as per clause 16.1 the Letter Grades awarded to the students in the each course shall be announced on the departmental notice board after duly approved by the Controller of Examinations. In case any student feels aggrieved, he/she can apply for revaluation after paying the prescribed fee for the purpose, within two weeks from the commencement of the semester immediately following the announcement of results. A committee will be constituted by the Controller of Examinations comprising the Chairperson of the concerned Class Committee (Convener), the teacher concerned and another teacher of the department who is knowledgeable in the concerned course. If the Committee finds that the case is genuine, it may jointly revalue the answer script and forward the revised mark to the Controller of Examinations with full justification for the revision if any.

17.2 The **"U"** grade once awarded stays in the grade sheet of the students and is not deleted when he/she completes the course successfully later. The grade acquired by the student later will be indicated in the grade sheet of the appropriate semester.

18.0 COURSE REPETITION AND ARREARS EXAMINATION

18.1 A student should register to re-do a core course wherein "I" or "W" grade is awarded. If the student is awarded "I", or "W" grade in an elective course either the same elective course may be repeated or a new elective course may be taken.

18.2 A student who is awarded "U" grade in a course shall write the end-semester examination as arrear examination , at the end of the next semester, along with the regular examinations of next semester courses. **The marks earned earlier in the continuous assessment tests for the course, will be used for grading along with the marks earned in the end-semester arrear examination for the course.**

19.0 GRADE SHEET

19.1 The grade sheet issued at the end of the semester to each student will contain the following:

(i) the credits for each course registered for that semester.

(ii) the performance in each course by the letter grade obtained.

(iii) the total credits earned in that semester.

(iv) the Grade Point Average (GPA) of all the courses registered for that semester and the Cumulative Grade Point Average (CGPA) of all the courses taken up to that semester.

19.2 The GPA will be calculated according to the formula

$$GPA = \frac{\sum_i (Ci)(GPi)}{\sum_i Ci}$$

where C_i is the number of credits assigned for i^{th} course
GP_i - Grade point obtained in the i^{th} course
For the cumulative grade point average (CGPA) a similar formula is used except that the sum is over all the courses taken in all the semesters completed up to the point in time.

I and W grades will be excluded for GPA calculations.

U, I and W grades will be excluded for CGPA calculations.

19.3 Classification of the award of degree will be as follows:

CGPA	Classification
8.50 and above, having completed in first appearance in all courses	First class with Distinction
6.50 and above, having completed within a period of 2 semesters beyond the programme period.	First Class
All others	Second Class

However, to be eligible for First Class with Distinction, a candidate should not have obtained U or I grade in any course during his/her study and should have completed the P.G. Programme within a minimum period covered by the minimum duration (clause 3.1) plus authorized break of study, if any (clause 8). To be eligible for First Class, a candidate should have passed the examination in all courses within the specified minimum number. of semesters reckoned from his/her commencement of study plus two semesters. For this purpose, the authorized break of study will not be counted. The candidates who do not satisfy the above two conditions will be classified as second class. For the purpose of classification, the CGPA will be rounded to first decimal place. For the purpose of comparison of performance of candidates and ranking, CGPA will be considered up to three decimal places.

20 ELIGIBILITY FOR THE AWARD OF THE MASTERS DEGREE

20.1 A student shall be declared to be eligible for the award of the Masters Degree, if he/she has:

i) registered for and undergone all the core courses and completed the Project Work,

ii) successfully acquired the required credits as specified in the Curriculum corresponding to his/her programme within the stipulated time,

iii) successfully completed the field visit/industrial training, if any, as prescribed in the curriculum.

iv) has no dues to the Institution, Hostels and Library.

v) no disciplinary action is pending against him/her

20.2 The award of the degree must be approved by the University.

21.0 POWER TO MODIFY:

Notwithstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

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M.TECH. (VLSI & EMBEDDED SYSTEMS)
CURRICULUM

SEMESTER I

Code No	Course Title	L	T	P	C	TC
MA 681	Applied Mathematics for Electronic Engineers	3	1	0	4	
EC 621	Advanced Digital System Design	3	0	0	3	
EC 622	VLSI design methodologies	3	0	0	3	
EC 623	Real Time Operating System	3	1	0	4	
	Elective - I	3	0	0	3	
	Elective - II	3	0	0	3	
Practical						
EC 624	VLSI Design Lab	0	0	3	1	

TOTAL CREDITS 21

SEMESTER II

Code No	Course Title	L	T	P	C	TC
EC 625	ASIC Design	3	0	0	3	
EC 626	Design of Embedded Systems	3	0	0	3	
EC 627	Advanced Embedded Systems	3	0	0	3	
EC 628	Embedded Networking	3	0	0	3	
	Elective - III	3	0	0	3	
	Elective - IV	3	0	0	3	
Practical						
EC 629	Embedded Systems Lab	0	0	3	1	

TOTAL CREDITS **19**

SEMESTER III

Code No	Course Title	L	T	P	C	TC
EC 721	Testing of VLSI circuits	3	0	0	3	
	Elective V	3	0	0	3	
	Elective VI	3	0	0	3	
Practical						
EC 722	Project work (Phase I)	0	0	12	6*	
					TOTAL CREDITS	**9**

SEMESTER IV

Code No	Course Title	L	T	P	C	TC
EC 722	Project work (Phase II)	0	0	35	18*	
	TOTAL	-	-	-	24	
					TOTAL CREDITS	**73**

* Credits for Project work (Phase I) of III Semester will be accounted along with project work (Phase II) of IV Semester

LIST OF ELECTIVE COURSES

Course Code	Course	L	T	P	C
ECY 101	VLSI signal processing	3	0	0	3
ECY 102	Low power VLSI Design	3	0	0	3
ECY 103	RF System Design	3	0	0	3
ECY 104	Advanced Microprocessors & Micro controllers Design	3	0	0	3
ECY 105	CAD for VLSI circuits	3	0	0	3
ECY 106	Reconfigurable Computing	3	0	0	3
ECY 107	Optimization techniques and their applications in VLSI design	3	0	0	3
ECY 108	RISC Processor Architecture and Programming	3	0	0	3
ECY 109	Signal integrity for High Speed Design	3	0	0	3
ECY 110	Soft Computing Techniques	3	0	0	3
ECY 111	Introduction to MEMS System Design	3	0	0	3
ECY 112	Application of MEMS Technology	3	0	0	3
ECY 113	Distributed Embedded Computing	3	0	0	3
ECY 114	CMOS mixed signal circuit design	3	0	0	3
ECY 115	Design of Semiconductor Memories	3	0	0	3
ECY 116	Controller Area Network	3	0	0	3
EC 608	Advanced Digital Signal Processing	3	1	0	4
ECY 001	Digital Image Processing	3	0	0	3
ECY 118	Wireless and Mobile Networks	3	0	0	3

M.TECH. (VLSI & EMBEDDED SYSTEMS)

SEMESTER I

MA 681 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L	T	P	C
3	1	0	4

OBJECTIVIE

The course is designed with a purpose of developing mathematical skills to understand and solve the problems of analytical subjects in the respective engineering streams.

UNIT-1 LINEAR ALGEBRAIC EQUATIONS AND EIGEN VALUE PROBLEM **9**

System of Equations – Solution by Gauss Elimination, Gauss-Jordon and LU decomposition method – Jacobi, Gauss-Seidal iteration method – Eigen values of a matrix by Jocobi and Power methods.

UNIT-2 WAVE EQUATION **9**

Solution of initial and boundary value problems-Characteristics-D'Alembert's Solution –Significance of characteristic curves - Laplace transform solution for displacement in a long string – a long string under its weight-Longitudinal vibration of a elastic bar with prescribed force on one end - free vibrations of a string.

UNIT-3 SPECIAL FUNCTIONS **9**

Bessel's equation - Bessel Functions - Legendre's equation - Legendre polynomials -Rodrigue's formula - Recurrence relations - generating functions and orthogonal property of Bessel function and Legendre Polynomials.

UNIT- 4 RANDOM VARIABLES **9**

One dimensional Random Variables - Moments and MGF - Binomial, Poisson Geometrical, Uniform, Exponential, Normal and Weibull distributions – Two - dimensional Random Variables – Marginal and Conditional distribution – Covariance and Correlation coefficient – Functions of one-dimensional and two - dimensional Random Variables.

UNIT-5 QUEUING THEORY **9**

Single and Multiple serve Markovian queuing models-Steady state system

size probabilities – Little's formula – Customer impatience – Priority quences - M/G/1 queuing system - P-K formula.

L-45, T-15

Total : 60 Periods

REFERENCES

1. Jain M.K., Iyengar .S.R.K: & Jain.R.K, "Numerical Methods for Scientific and Engg., Computation", New Age International (P) Ltd, Publishers, 2003.
2. Sankara Rao K., "Introduction to Partial Differential Equation", Prentice Hall of India, 1997.
3. Grewal B.S, "Higher Engg. Mathematics", Khanna Publishers, 2005.
4. Kapur J.N & Saxena. H.C, "Mathematical Statistics", S. Chand & Company Limited, New Delhi, 2003.
5. Taha H.A, " Operations Research – An Introduction",Prentice Hall of India, 2001.
6. Gross.D & Harris.C.M, "Fundamentals of Queuing Theory", John Wiley & Sons, 1985.

OUTCOME

- Students will be in a position to apply correct method to solve a given problems. The approaches they have undergone will provide them hands on experience for doing their project work.
- They understand pretty well the implications of mathematics they have studied in their core subjects like advanced digital signal processing, communication network, image processing and so on.
- The special functions give the best of solutions for the complicated homogeneous differential equations with variable constants in power series. The special functions are used in the expansion of arbitrary functions in a series analogous to expansion of arbitrary function in fourier series.

EC621 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE

To learn

- Design and analysis of sequential circuits
- Testing & fault diagnosis and its algorithms
- Design using programmable logic devices

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modelling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Array

UNIT V NEW GENERATION PROGRAMMABLE LOGIC DEVICES 9

Foldback Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM –

Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

L – 45

Total – 45 Periods

REFERENCES

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, “Fundamentals of Digital Logic with VHDL Deisgn”, Tata McGraw Hill, 2002.
3. Mark Zwolinski, “Digital System Design with VHDL”, Pearson Education, 2004.
4. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
5. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.
6. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
7. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.

OUTCOME

On completion of the course, students will be knowledgeable in

- Design and analysis of sequential circuits.
- Analyzing faults in circuits.
- Design of sequential circuits using programmable devices.

EC 622 VLSI DESIGN METHODOLOGIES L T P C
3 0 0 3

OBJECTIVE

To learn

- The conceptual view of CMOS circuits and VLSI design flow
- VLSI system components circuits and analog VLSI
- Synthesis of digital VLSI systems from register-transfer level descriptions using Verilog HDL.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, CMOS fabrication and layout, VLSI design flow, MOS transistor theory, CMOS technologies, CMOS process enhancement, DC and transient characteristics, switching times, Super buffers, driving large capacitance loads, Static CMOS design, dynamic CMOS design

UNIT II CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing, Scaling.

UNIT III VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution

UNIT IV ANALOG VLSI 9

Introduction to analog VLSI, Advanced MOS modeling, BJT modeling, CS, CD and CG amplifiers, Current mirrors-active loads, high input impedance current mirrors, BJT gain stages, CMOS operational amplifiers-compensation, comparators, sample and hold circuits.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Introduction to logic design with verilog HDL, hierarchical modeling concepts,

logic design with behavioral models of combinational and sequential logic, synthesis of combinational and sequential logic, post synthesis design tasks-design validation - timing verification – elimination of ASIC timing violations-system task for timing verification-fault simulation and testing.

TOTAL: 45 Periods

REFERENCES

1. Neil H.E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design”, Pearson Education Asia, 2nd edition, 2000.
2. John P.Uyemura, “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
3. D.A.John & K.Martin, “Analog Integrated Circuit Design”, Wiley, 1997.
4. Mohamed Ismail, Terri Fiez, “Analog VLSI signal and information processing”, McGraw Hill International Editions, 1994.
5. Michael D.Ciletti, “Advanced digital design with the Verilog HDL”,PHI, 2003.
6. Eugene D.Fabricious, “Introduction to VLSI Design”, McGraw Hill International Editions, 1990.
7. Wayne Wolf, “Modern VLSI Design System on chip”. Pearson Education.2002.

OUTCOME

On completion of the course, students will be knowledgeable

- Modeling of analog and digital VLSI systems
- Simulation and Synthesis of digital VLSI systems using hardware description language.

EC623 REAL TIME OPERATING SYSTEMS L T P C
3 1 0 4

OBJECTIVE

To learn

- Basic concepts Operating Systems, Real-time systems and Real-time Operating Systems
- Design and analysis of computer systems for real-time applications.
- Resource management, time-constrained communication, scheduling and imprecise computations, real-time kernels.

UNIT I REVIEW OF OPERATING SYSTEMS 9

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling.

UNIT II OVERVIEW OF RTOS 9

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks

UNIT III REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV REAL TIME KERNEL 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V RTOS APPLICATION DOMAINS 9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

L – 45, T – 15,
Total – 60 Periods

REFERENCES

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
2. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
3. Charles Crowley, “Operating Systems-A Design Oriented approach”, McGraw Hill 1997.
4 C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.
5. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999.
6. Mukesh Sighal and N. G. Shi “Advanced Concepts in Operating System”, McGraw Hill 2000.

OUTCOME

On completion of the course, students will be knowledgeable in

- Real-time embedded systems and various real-time operating systems.
- Identifying variable faults in Embedded systems.

EC624 **VLSI DESIGN LAB** **L T P C**
0 0 3 1

OBJECTIVE

To get hands on experience on Analog and Digital IC/ASIC design using Mentor Graphics and Tanner Tools.

FPGA BASED EXPERIMENTS:

1. Design Entry Using Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.

ASIC BASED EXPERIMENTS:

1. ASIC RTL realization- Tanner
2. Interpretation of standard cell library descriptions, Boolean optimization, optimization for area, power – Mentor Graphics
3. Static Timing analyses procedures and constraints. Critical path considerations – Mentor Graphics
4. Scan chain insertion, Floor Planning Routing and Placement procedures and alternatives. Back annotation, layout generation, LVS, Formal verification – Mentor Graphics
5. Layout generation for analog circuit modules- Mentor Graphics /TANNER
6. LVS, Back annotation- TANNER/ Mentor Graphics

OUTCOME

On completion of the course, students will be knowledgeable in

- Development of digital integrated circuits design, implementation methodologies and testing.
- Back-end design flow of Digital and Analog integrated circuits.

SEMESTER II

EC625	ASIC DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVE

To Learn

- The concept of semicustom and programmable ASIC types.
- The fundamentals of digital logic design and the physical features of each ASIC.
- ASIC logic design, testing of physical design partitioning, floor planning, placement, and routing.

UNIT I INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort – Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICs, LOGIC CELLS AND I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT & ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL : 45 Periods

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991 3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Vranesic, “Field Programmable Gate Arrays”, Kluwer Academic Publishers, 1992.
3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
4. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

OUTCOME

On completion of the course, students will be knowledgeable in

- The ASIC Design Flow and its Architecture.
- The Logic Synthesis and Testing methodologies.
- Floor Planning and Physical Design Flows.

EC626 DESIGN OF EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVE

To learn

- Embedded product design covering various dimensions of product development, Quality principles, Project Management and discussion with suitable case study.
- Co-synthesis of Embedded hardware and software.

UNIT I EMBEDDED DESIGN LIFE CYCLE 9

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT II PARTITIONING DECISION 9

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System start-up – Hardware manipulation – memory mapped access – speed and code density.

UNIT III INTERRUPT SERVICE ROUTINES 9

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyzer – Caches – Computer optimization – Statistical profiling.

UNIT IV IN-CIRCUIT EMULATORS 9

Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT V TESTING 9

Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

TOTAL-45 Periods

REFERENCE

1. Arnold S. Berger – “Embedded System Design: An introduction to processor, tools and techniques”, CMP books, USA 2002.
2. Sriram Iyer, “Embedded Real time System Programming”, Tata McGraw Hill, 2003.
3. Arkin, R.C., “Behaviour-based Robotics”, MIT Press, 1998.
4. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006. 5. Herma K.

OUTCOME

On completion of the course, students will be knowledgeable in

- The quality principles and tools in product development process.
- The division of hardware/software in embedded systems.
- Various testing methodologies during the product development cycle.

EC627 ADVANCED EMBEDDED SYSTEMS L T P C
3 0 0 3

OBJECTIVE

To learn

- Basics of Embedded hardware and software
- System modelling and Co-synthesis of Embedded Systems.
- Various memory types and Interfacing Techniques.

UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE 9

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Interrupt routines in an RTOS environment.

UNIT II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9

Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modelling- Single-processor Architectures & Multi-Processor Architectures, comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modelling, Formulation of the HW/SW scheduling, Optimization.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV MEMORY AND INTERFACING 9

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9

Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology – Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

L – 45
Total – 45 Periods

REFERENCES

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.
2. Tammy Noergaard, ”Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006.
3. Raj Kamal, “Embedded Systems- Architecture, Programming and Design”, Tata McGraw Hill, 2006.
4. Frank Vahid and Tony Givargis ‘Embedded Systems Design: A Unified Hardware/Software Introduction’, John & Wiley Publications, 2002.
5. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
6. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
7. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
8. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann Publishers, 2001.

OUTCOME

On completion of the course, students will be knowledgeable in

- Hardware software co design and its issues.
- Hardware software partitioning and its concurrent design.

EC628 EMBEDDED NETWORKING **L T P C**
3 0 0 3

OBJECTIVE

To learn

- Various Serial and parallel communication protocols.
- USB and CAN Bus protocols
- Ethernet fundamentals and usage in Embedded Networking

UNIT I EMBEDDED COMMUNICATION PROTOCOLS 9

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming -ISA/PCI Bus protocols – Firewire.

UNIT II USB AND CAN BUS 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors – PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

UNIT III ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol

UNIT IV EMBEDDED ETHERNET 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V WIRELESS EMBEDDED NETWORKING 9

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TOTAL= 45 Periods

REFERENCE

1. Frank Vahid, Tony Givargis 'Embedded Systems Design: A Unified Hardware/ Software Introduction', John & Wiley Publications,2002
2. Jan Axelson, 'Parallel Port Complete:Programming, interfacing and using the PC's parallel printer port', Penram publications, 1996.
3. Dogan Ibrahim, 'Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series', Elsevier 2008.
4. Jan Axelson 'Embedded Ethernet and Internet Complete', Penram publications, 2003.
5. Bhaskar Krishnamachari, 'Networking Wireless Sensors', Cambridge press 2005.

OUTCOME

On completion of the course, students will be knowledgeable in

- Various communication protocols in Embedded Networking.
- Basic concepts of wireless sensor networks and its MAC protocols.

EC629 EMBEDDED SYSTEMS LAB

L	T	P	C
0	0	3	1

OBJECTIVE

- To get hands on training on Embedded tools.
- To develop the various applications using 8051 Microcontroller, PIC controller & ARM processor.

LIST OF EXPERIMENTS :

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers- Assembly and C Programming: I/O Programming, Timers,
2. Interrupts, Serial port programming with 8051/PIC Microcontrollers- Assembly and C programming
3. PWM Generation, Motor Control, ADC/DAC with 8051/PIC Microcontrollers- Assembly and C programming
4. LCD and RTC Interfacing, Sensor Interfacing with 8051/PIC Microcontrollers- Assembly and C programming
5. Design with 16 bit processors: I/O programming, Timers, Interrupts, Serial Communication
6. Design with ARM Processors: I/O programming, ADC/DAC, Timers, Interrupts
7. Study of one type of Real Time Operating Systems (RTOS)
8. Simple wired/wireless network simulation using NS2 software
9. Programming of TCP/IP protocol stack.

OUTCOME

At the end of the course the student will be able to

- Program and Debug various applications using Keil µVision, IAR embedded workbench and MPlab tools.

Semester III

EC721 TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- Automated and manual techniques for generating tests for faults in digital circuits and systems.
- Generation of test vectors for combinational and sequential circuits
- Fault diagnosis algorithms

UNIT I BASICS OF TESTING AND FAULT MODELING 9

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design – System level DFT approaches.

UNIT IV SELF TEST AND TEST ALGORITHMS 9

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

L – 45,
Total – 45 Periods

REFERENCES:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L. Crouch, "Design Test for Digital ICs and Embedded Core Systems", Prentice Hall International, 2002.

OUTCOME

On completion of the course, students will be knowledgeable in

- Principles of testing digital systems.
- Design for testability in combinational and sequential circuits.
- Basics of self test and fault diagnosis.

ELECTIVES

ECY101 VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn.

- Fundamentals of pipelining and parallel processing on FIR and IIR filters
- The concepts of retiming, unfolding, transforms and rank order filters.
- Different bit level architectures and their complexities
- The general architecture, features of DSP and need for low power VLSI design.

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties; Unfolding – algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff

noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL : 45 Periods

REFERENCES

1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

OUTCOME

On completion of the course, students will be knowledgeable in

- Various algorithms to design application specific VLSI architecture
- Analyzing different number representations, arithmetic based binary representations.
- Architecture of Low power Digital signal Processors.

ECY102 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- The Power analysis used in CMOS devices.
- Various techniques to reduce the power consumption in VLSI Circuits.
- Various Low power Architectures.

UNIT I DEVICE & TECHNOLOGY IMPACT ON LOW POWER 9

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT II SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS 9

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation -Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT III LOW POWER DESIGN 9

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre computation logic

UNIT IV LOW POWER ARCHITECTURE & SYSTEMS, LOW POWER CLOCK DISTRIBUTION 9

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design- Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co-design of clock network

UNIT V ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES 9

Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis.

TOTAL : 45 Periods

REFERENCES

1. Gary K. Yeap, Farid N. Najm, “Low power VLSI design and technology”, World Scientific Publishing Ltd., 1996.
2. Dimitrios Soudris, Christian Piguet, Costas Goutis,” Designing CMOS circuits for low power”,Kluwer Academic Publishers,2002
3. Kaushik Roy and Sharat C. Prasad,"Low-Power CMOS VLSI Circuit Design" ,Wiley-Interscience, 2000.
4. Chandrakasan, R. Brodersen, “CMOS Low Power Digital Design”, Kluwer Academic Publications. 1995.
5. Rabaey, M. Pedram, “Low Power Design Methodologies”, Kluwer Academic Publications. 1996.
6. Christian Piguet, “Low-power CMOS circuits: technology, logic design and CAD tools”, CRC Press, Taylor & Francis Group, 2006.

OUTCOME

On completion of the course, students will be knowledgeable in

- Static and dynamic power dissipation in integrated chips.
- Estimation of power for simple models.
- Low Power Dissipation Techniques in Clocking strategies, I/O circuits

ECY103	RF SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVE

To Learn

- The importance of RF design
- Basics of filter design, RF components and RF oscillators
- The applications of RF design

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES **9**

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS **9**

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS **9**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

UNIT IV PLL AND FREQUENCY SYNTHESIZERS **9**

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer- N frequency synthesizers, Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS **9**

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier

based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

TOTAL : 45 Periods

REFRENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

OUTCOME

On completion of the course, students will be knowledgeable in

- Behavior of RF components, Realization of filters
- Characteristics and applications of RF circuits

ECY104 ADVANCED MICROPROCESSORS & MICRO CONTROLLERS DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- The Architecture of RISC and CISC Processors and controllers.
- Programming models of RISC and CISC processors.

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction set - Data formats - Instruction formats - Addressing modes - Memory Hierarchy - register file - Cache - Virtual memory and paging - Segmentation - Pipelining - The instruction pipeline - pipeline hazards - Instruction level parallelism - reduced instruction set - Computer principles - RISC versus CISC - RISC properties - RISC evaluation - On-chip register files versus cache evaluation.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

The software model - functional description - CPU pin descriptions - RISC concepts - bus operations - Super scalar architecture - pipe lining - Branch prediction - The instruction and caches - Floating point unit - protected mode operation - Segmentation - paging - Protection - multitasking - Exception and interrupts - Input/Output - Virtual 8086 model - Interrupt processing - Instruction types - Addressing modes - Processor flags - Instruction set - Basic programming the Pentium Processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE 9

ARM: The ARM architecture - ARM organization and implementation - The ARM instruction set - The thumb instruction set - Basic ARM Assembly language program - ARM CPU cores.

UNIT IV MOTOROLA 68HC11 MICRO CONTROLLER 9

Instructions and addressing modes - operating modes - Hardware reset - Interrupt system - Parallel I/O ports - Flats - Real time clock - Programmable timer - pulse accumulator - serial communication interface - A/D converter - hardware expansion - Basic Assembly Language programming.

UNIT V PIC MICRO CONTROLLER 9

CPU Architecture - Instruction set - Interrupts - Timers - Memory - I/O port expansion - I2C bus for peripheral chip access - A/D converter - UART.

TOTAL : 45 Periods

REFERENCES

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill. Inc., 1995.
2. James L. Antonakos, "The Pentium Microprocessor", Pearson Education, 1997.
3. Steave Furber, "ARM system - on - chip architecture", Addison Wesley, 2000.
4. John.B..Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
5. Gene. H.Miller, "Micro Computer Engineering", Pearson Education, 2003.
6. James L Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson education, 1999.
7. Barry B. Brey, "The Intel Microprocessors Architecture, Programming and Interfacing", PHI, 2002.

OUTCOME

On completion of the course, students will be knowledgeable in

- Functionality of advanced Microprocessors and Microcontrollers
- Writing programs in PENTIUM, ARM, MOTOROLA and PIC.

ECY105 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVE

To Learn

- VLSI layout design rules and translate circuit concepts onto silicon
- Floor planning concepts in back end designs.

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL : 45 Periods

REFERENCE

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.

2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

OUTCOME

On completion of the course, students will be knowledgeable in

- Identifying the best approach algorithm to optimize circuits at different levels of design.
- Applying the algorithms in the back end flow to optimize the circuits for maximum speed and area.

EC106 RECONFIGURABLE COMPUTING **L T P C**
3 0 0 3

OBJECTIVE

To Learn

- Basic concepts of Reconfigurable computing
- Various Reconfigurable architectures and their applications.

UNIT I INTRODUCTION **9**

Goals and motivations - History, state of the art, future trends - Basic concepts and related fields of study - Performance, power, and other metrics - Algorithm analysis and speedup projections - RC Architectures - Device characteristics - Fine-grained architectures - Coarse-grained architectures.

UNIT II FPGA DESIGN **9**

FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT III PARALLEL PROCESSING **9**

RC Application Design - Parallelism - Systolic arrays -Pipelining - Optimizations -Bottlenecks - High-level Design - High-level synthesis - High-level languages - Design tools.

UNIT IV ARCHITECTURES **9**

Hybrid architectures- Communication - HW/SW partitioning - Soft-core microprocessors- System architectures -System design strategies - System services - Small-scale architectures - HPC architectures - HPEC architectures - System synthesis - Architectural design space explorations.

UNIT V CASE STUDY **9**

Case Studies- Signal and image processing - Bioinformatics - Security - Special Topics - Partial Reconfiguration - Numerical Analysis -Performance Analysis/ Prediction - Fault Tolerance

TOTAL :45 Periods

REFERENCES:

1. C. Maxfield, “The Design Warrior's Guide to FPGAs: Devices, Tools and flows”, Newnes, 2004.
2. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
3. C. Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2007.
4. P. Lysaght and W. Rosenstiel, “New Algorithms, Architectures and Applications for Reconfigurable Computing”, Springer, 2005.
5. D. Pellerin and S. Thibault, “Practical FPGA Programming in C”, Prentice-Hall, 2005.
6. W. Wolf, “FPGA Based System Design”, Prentice-Hall, 2004.
7. R. Cofer and B. Harding, “Rapid System Prototyping with FPGAs: Accelerating the Design Process”, Newnes, 2005.

OUTCOME

On completion of the course, students will be knowledgeable in

- Various RC architectures and its characteristics
- FPGA design and logic minimization techniques
- Parallel Processing and Pipelining architectures

ECY107	OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVE

To Learn

- The Statistical Modeling and various techniques of Test Generation Patterns.
- Placement & Power Estimation and convex optimization techniques.
- Statistical analysis methods and fundamentals of genetic algorithms.

UNIT I STATISTICAL MODELING **9**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS **9**

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT III CONVEX OPTIMIZATION **9**

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max- monomial fitting, Polynomial fitting.

UNIT IV GENETIC ALGORITHM **9**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation-Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFR- Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION 9

Global routing-FPGA technology mapping-circuit generation-test generation in a GA framework-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL : 45 Periods

REFERENCES

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI:Timing and Power”, Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design,Layout and test Automation”, Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University Press, 2004.

OUTCOME

On completion of the course, students will be knowledgeable in

- Optimization techniques to improve the implementation of VLSI designs.
- Genetic algorithm to solve problems.
- Statistical modeling in one or more disciplines.

ECY108	RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVE

To Learn

- The advanced processor family architectures like AVR and ARM Processors
- Assembly language programming and applications of ARM Processor

UNIT I AVR MICROCONTROLLER ARCHITECTURE 9

Architecture – memory organization – addressing modes – instruction set – programming techniques –Assembly language & C programming- Development Tools – Cross Compilers – Hardware Design Issues .

UNIT II PERIPHERAL OF AVR MICROCONTROLLER 9

I/O Memory – EEPROM – I/O Ports –SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing .

UNIT III ARM ARCHITECTURE AND PROGRAMMING 9

Arcon RISC Machine – Architectural Inheritance – Core & Architectures - Registers – Pipeline - Interrupts – ARM organization - ARM processor family – Co-processors. Instruction set – Thumb instruction set – Instruction cycle timings - The ARM Programmer's model – ARM Development tools – ARM Assembly Language Programming and "C" compiler programming.

UNIT IV ARM APPLICATION DEVELOPMENT 9

Introduction to DSP on ARM –FIR Filter – IIR Filter – Discrete fourier transform – Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Example: Standalone - Embedded Operating Systems – Fundamental Components - Example Simple little Operating System

UNIT V DESIGN WITH ARM MICROCONTROLLERS 9

Integrated development environment – Standard I/O Libraries - User Peripheral Devices – Application of ARM processor: Wireless Sensor Networks, Robotics.

TOTAL : 45 Periods

REFERENCES

1. Steve Furber, “ARM system on chip architecture”, Addison Wesley, 2000.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier 2007.
3. Trevor Martin, “The Insider's Guide To The Philips ARM7-Based Microcontrollers - An Engineer's Introduction To The LPC2100 Series” Hitex (UK) Ltd.,
4. Dananjay V. Gadre, “Programming and Customizing the AVR microcontroller”, McGrawHill 2001 5. ARM Architecture Reference Manual 6. LPC213x User Manual

OUTCOME

On completion of the course, students will be knowledgeable in

- AVR and ARM architectures and programming in both assembly language and C language
- Various tools like WinAVR and IAR Embedded workbench to develop the miniproject using AVR and ARM processors.

ECY 109 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- Analyzing high-speed circuits with signal behavior modeling.
- Signal integrity concepts
- Analyze signal measurements and make trade off decisions based on signal budget and design requirements.

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations - L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (stipline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths - gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses - Rs, tan, routing parasitic, Common-mode current, differential-mode current, Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL =45 Periods

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity - Simplified , Prentice Hall PTR, 2003.

OUTCOME

On completion of the course, students will be knowledgeable in

- Signal behaviour on high speed ciruits such as cross talk in transmission lines
- Power considerations and timing analysis and other losses in system design
- Measurements in clock oscillators

ECY110 SOFT COMPUTING TECHNIQUES

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- Fuzzy sets, fuzzy logic and use of heuristics based on human experience
- Neural networks to generalize appropriate rules for inferencing systems
- Mathematical background for carrying out the optimization associated with neural networks
- The genetic algorithms and other random search procedures for self-learning situations

UNIT I INTRODUCTION **9**

Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

UNIT II ARTIFICIAL NEURAL NETWORK **9**

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

UNIT III FUZZY LOGIC SYSTEM **9**

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear timedelay system.

UNIT IV GENETIC ALGORITHM **9**

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and anD-colony search techniques for solving optimization problems.

UNIT V APPLICATIONS 9

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox. Stability analysis of Neural-Network interconnection systems. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

TOTAL : 45 Periods

REFERENCES

1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing House, 1999.
2. Kosko,B. "Neural Networks And Fuzzy Systems", Prentice-Hall of India Pvt. Ltd., 1994.
3. Klir G.J. & Folger T.A. "Fuzzy sets, uncertainty and Information", Prentice-Hall of India Pvt. Ltd., 1993.
4. Zimmerman H.J. "Fuzzy set theory-and its Applications"-Kluwer Academic Publishers, 1994.
5. Driankov, Hellendroon, "Introduction to Fuzzy Control", Narosa Publishers.

OUTCOME

On completion of the course, students will be knowledgeable in

- Developing systems that encapsulate human expertise.
- Applications of soft computing techniques in Biomedical Application, Intelligent Instrumentation, Defense Application, Fault Tolerance System, Critical application areas.

ECY 111 INTRODUCTION TO MEMS SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE

This course is an introduction to MEMS, which also uses micro electronics. This course fulfils the need of electronic engineer who wants to create MEMS devices in the field of Mechanical, Electronic Sensors, Optical and RF system.

UNIT I INTRODUCTION TO MEMS **9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication.

UNIT II MECHANICS FOR MEMS DESIGN **9**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics - actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN **9**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES **9**

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies - Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS **9**

Optical MEMS - System design basics - Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS - design basics, case study - Capacitive RF MEMS switch, performance issues.

TOTAL : 45 Periods

REFERENCES

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000.
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton, 2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

OUTCOME

At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

ECY 112 APPLICATIONS OF MEMS TECHNOLOGY

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn,

- The principles of micro-fabrication to the development of micromechanical devices and the design of Microsystems.
- The principles of energy transduction, sensing and actuation on a microscopic scale.
- Modeling and Analysis of micro electromechanical devices and systems.

UNIT I MEMS: MICRO-FABRICATION, MATERIALS AND ELECTRO MECHANICAL CONCEPTS **9**

Overview of micro fabrication - Silicon and other material based fabrication processes - Concepts: Conductivity of semiconductors-Crystal planes and orientation-stress and strain-flexural beam bending analysis-torsional deflections-Intrinsic stress- resonant frequency and quality factor.

UNIT II ELECTROSTATIC SENSORS AND ACTUATION **9**

Principle, material, design and fabrication of parallel plate capacitors as lectrostatic sensors and actuators-Applications

UNIT III THERMAL SENSING AND ACTUATION **9**

Principle, material, design and fabrication of thermal couples, thermal bimorph sensors, thermal resistor sensors-Applications.

UNIT IV PIEZOELECTRIC SENSING AND ACTUATION **9**

Piezoelectric effect-cantilever piezo electric actuator model-properties of piezoelectric materials- Applications.

UNIT V CASE STUDIES **9**

Piezo resistive sensors, Magnetic actuation, Micro fluids applications, Medical applications, Optical MEMS.

TOTAL : 45 Periods

REFERENCES

1. Chang Liu, "Foundations of MEMS", Pearson International Edition, 2006.
2. Marc Madou , "Fundamentals of microfabrication",CRC Press, 1997.
3. Boston , "Micromachined Transducers Sourcebook",WCB McGraw Hill, 1998.
4. M.H.Bao "Micromechanical Transducers :Pressure sensors, accelerometers and gyroscopes", Elsevier, Newyork, 2000.

OUTCOME

- At the end of this course, the student will have knowledge on MEMS materials, fabrication and their applications.

ECY113 DISTRIBUTED EMBEDDED COMPUTING **L T P C**

3 0 0 3

OBJECTIVE

To Learn

- The various hardware and software architectures used for distributed embedded computing.
- Distributed computing system models and Distributed databases.
- The infrastructure required to support an Internet connection, uses of common Internet protocols, and basic principles of the DNS.
- The distributed computing technologies

UNIT I THE HARDWARE INFRASTRUCTURE **9**

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – wide Area Networks – Network management – Network Security – Cluster computers.

UNIT II INTERNET CONCEPTS **9**

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III DISTRIBUTED COMPUTING USING JAVA **9**

I/O streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT IV EMBEDDED AGENT **9**

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V EMBEDDED COMPUTING ARCHITECTURE **9**

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL: 45 Periods

REFERENCES

1. Dietel & Dietel, “JAVA-How to program”, Prentice Hall 1999.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – Concepts and Design”, Addison Wesley 1988.
4. Bernd Kleinjohann “Architecture and Design of Distributed Embedded Systems”, C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

OUTCOME

On completion of the course, students will be knowledgeable in

- Designing and analyzing high-performance computer system.
- Selecting the suitable embedded architecture.

ECY114 CMOS MIXED SIGNAL CIRCUIT DESIGN L T P C

3 0 0 3

OBJECTIVE

To learn

- The Basic concepts of advanced MOS and bipolar analog and mixed-signal integrated circuits.
- The concepts of PLL, Sampling circuits and Filters.

UNIT I PLL AND SWITCHED CAPACITOR CIRCUITS 9

Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL- Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

UNIT II SAMPLING CIRCUITS 9

Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT III DAC 9

Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

UNIT IV ADC 9

Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures, pipelined architectures, Successive approximation architectures, interleaved architectures.

UNIT V FILTERS **9**

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

TOTAL: 45 Periods

REFERENCE:

1. Razavi, "Design of analog CMOS integrated circuits", McGraw Hill, 2001
2. Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2002
4. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley & Sons
5. Baker, Li, Boyce, "CMOS : Circuit Design, layout and Simulation", PHI, 2000

OUTCOME

On completion of the course, students will be able to:

- Design analog circuits on state-of-the-art mixed-signal CMOS VLSI for communications and signal processing applications.

ECY115 DESIGN OF SEMICONDUCTOR MEMORIES **L T P C**
3 0 0 3

OBJECTIVE:

To Learn

- The implementation methods and problems in designing and making semiconductor memories.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES **9**

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAM- Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NONVOLATILE MEMORIES **9**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS, PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE **9**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

UNIT IV RELIABILITY AND RADIATION EFFECTS **9**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT V PACKAGING TECHNOLOGIES 9

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs) -Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TOTAL: 45 Periods

REFERENCES

1. Ashok K.Sharma,"Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3. Betty Prince,“Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

OUTCOME

On completion of the course, students will be able to:

- Design MOS memories.
- Design memory fault modeling and memory design test-abilities.

ECY116 CONTROLLER AREA NETWORK L T P C
3 0 0 3

OBJECTIVE

To Learn

- Basic concepts of Embedded networking.
- CAN controller overview and Implementation.
- CAN Development Tools.

UNIT I EMBEDDED NETWORK REQUIREMENTS 9

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

UNIT II CAN OPEN 9

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

UNIT III CAN 9

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

UNIT IV IMPLEMENTATION OF CAN OPEN 9

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.

UNIT V ISSUES 9

Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

Total: 45 Periods

REFERENCES:

1. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.
2. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2005.
3. Mohammed Farsi, Barbosa, “CANopen Implementation : Applications to Industrial Networks (Industrial Control, Computers, and Communications Series,18),Research Studies Press,2000
4. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2007.

OUTCOME

On completion of this course, the students will understand,

- CAN message format
- CAN Implementation method and CAN Issues
- Identify the different types of noise commonly found in CAN.

EC 608 ADVANCED DIGITAL SIGNAL PROCESSING L T P C
(Common to M.Tech Communication Systems) 3 1 0 4

[Review of discrete-time signals and systems- DFT and FFT, Z-Transform, Digital Filters is recommended]

OBJECTIVE

- To understand the discrete time signals & systems and their analysis using various transforms.
- To learn the analysis and synthesis of IIR & FIR filters.
- To learn the basics of multirate DSP

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Autocovariance matrices. Parseval's Theorem, Wiener-Khintchine Relation- Power Spectral Density-Periodogram Spectral Factorization, Filtering random processes. Low Pass Filtering of White Noise.Parameter estimation: Bias and consistency.

UNIT II SPECTRUM ESTIMATION 9

Estimation of spectra from finite duration signals, Non-Parametric Methods-Correlation Method Periodogram Estimator, Performance Analysis of Estimators -Unbiased, Consistent Estimators- Modified periodogram, Bartlett and Welch methods, Blackman -Tukey method. Parametric Methods - AR, MA, ARMA model based spectral estimation. Parameter Estimation -Yule-Walker equations, solutions using Durbin's algorithm.

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear prediction- Forward and backward predictions, Solutions of the Normal equations- Levinson- Durbin algorithms. Least mean squared error criterion - Wiener filter for filtering and prediction, FIR Wiener filter and Wiener IIR filters,Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR). RLS adaptive filters-Exponentially weighted RLSsliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate - Interpolation and Decimation, Decimation by an nteger factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter mplementation for sampling rate conversion- direct form FIR structures, Polyphase filter structures, time-variant structures. Multistage implementation of multirate system. Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

L -45 T-15 Total- 60

REFERENCES

1. Monson H.Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc.,Singapore, 2002.
2. John G. Proakis, Dimitris G.Manolakis, Digital Signal Processing Pearson Education, 2002.
3. John G. Proakis et.al.,'Algorithms for Statistical Signal Processing', Pearson Education, 2002.
4. Dimitris G.Manolakis et.al.,'Statistical and adaptive signal Processing',McGraw Hill, Newyork, 2000.
5. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.(For Wavelet Transform Topic)

OUTCOME

After successful completion of the course, the students will be able

- To analyse and synthesize digital signals and systems using various transforms.
- To apply Wavelet Transform techniques in multirate DSP.

ECY001 DIGITAL IMAGE PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn

- Fundamentals and transforms for image processing.
- The image enhancement techniques
- Image restoration procedures.
- The image compression procedures.
- The image segmentation and representation techniques.

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals -RGB,HSI models, Image sampling, Quantization, dither, Two-dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms – DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, and Wavelet Transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic filters, Homomorphic filtering, Color image enhancement. Image Restoration –degradation model, Unconstrained and Constrained restoration, Inverse filtering – removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations – spatial transformations, Gray-Level interpolation.

UNIT IV IMAGE SEGMENTATION AND RECOGNITION 9

Edge detection. Image segmentation by region growing, region splitting and merging, edge linking.. Image Recognition – Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Back Propagation Neural Network, Neural Network applications in Image Processing.

UNIT V IMAGE COMPRESSION **9**

Need for data compression, Huffman,. Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT and Wavelet. JPEG, MPEG. Standards, Concepts of Context based Compression.

Total: 45

REFERENCES:

1. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
2. Anil K. Jain, 'Fundamentals of Digital Image Processing', Prentice Hall of India, 2002.
3. David Salomon : Data Compression – The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
4. Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
5. William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
6. Milman Sonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
7. Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.

OUTCOME

On completion of the course, students will gain knowledge

- On basic concepts of image processing and image transforms
- To apply the concepts of image segmentation, image classification to any image and find their performances.
- On different image enhancement and restoration models and techniques
- On the need for image compression and the concepts involved in it.

ECY 118 WIRELESS AND MOBILE NETWORKS

L	T	P	C
3	0	0	3

OBJECTIVE

To Learn,

- Fundamentals of wireless communications,
- Systems which operate on wireless principles.
- Routing protocols
- Transport layer and application layer

UNIT I INTRODUCTION **9**

Wireless Transmission - signal propagation - spread spectrum - Satellite Networks- Capacity Allocation - FAMA - DAMA - MAC

UNIT II MOBILE NETWORKS **9**

Cellular W ireless Networks - GSM - Architecture - Protocols - Connection Establishment - Frequency Allocation - Routing - Handover - Security - GPRA CDMA architecture

UNIT III WIRELESS NETWORKS **9**

Wireless LAN - IEEE 802.11 - IEEE 802.16 - Standard-Architecture – Services - AdHoc Network- Hiper Lan - Blue Tooth.

UNIT IV ROUTING **9**

Mobile IP - DHCP - AdHoc Networks - Proactive and Reactive Routing Protocols - Multicast Routing

UNIT V TRANSPORT AND APPLICATION LAYERS **9**

TCP over Adhoc Networks - WAP - Architecture - WWW Programming Model - WDP - WTLS - WTP - WSP - WAE - WTA Architecture - WML -WML scripts.

TOTAL : 45 PERIODS

REFERENCES

1. Kaveh Pahlavan, Prasanth Krishnamoorthy, "Principles of Wireless Networks PHI/Pearson Education, 2003
2. Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, "Principles of Mobile computing", Springer, New york, 2003.
3. C.K.Toh, "AdHoc mobile wireless networks", Prentice Hall, Inc, 2002.
4. Charles E. Perkins, "Adhoc Networking", Addison-Wesley, 2001.
5. Jochen Schiller, "Mobile communications", PHI/Pearson Education, Second Edition, 2003.
6. William Stallings, "Wireless communications and Networks", PHI/Pearson Education, 2002.

OUTCOME

On completion of this course, the students will understand,

- Fundamentals of Wireless communication such as Capacity allocation, wireless transmission, Spread spectrum techniques
- Architecture of Cellular and IP networks
- Routing in wireless and mobile networks
- Transport and application layer protocols.