UNIVERSITY VISION AND MISSION

VISION

B.S. Abdur Rahman Institute of Science & Technology aspires to be a leader in Education, Training and Research in Engineering, Science, Technology and Management and to play a vital role in the Socio-Economic progress of the Country.

MISSION

- To blossom into an internationally renowned University.
- To empower the youth through quality education and to provide professional leadership.
- To achieve excellence in all its endeavors to face global challenges.
- To provide excellent teaching and research ambience.
- To network with global Institutions of Excellence, Business, Industry and Research Organizations.
- To contribute to the knowledge base through Scientific enquiry, Applied Research and Innovation.

VISION AND MISSION OF THE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Department of Electronics and Communication Engineering envisions to be a leader in providing state of the art education through excellence in teaching, training, and research in contemporary areas of Electronics and Communication Engineering and aspires to meet the global and socio economic challenges of the country.

MISSION

- The Department of Electronics and Communication Engineering, endeavors to produce globally competent Engineers prepared to face challenges of the society.
- To enable the students to formulate, design and solve problems in applied science and engineering.
- To provide excellent teaching and research environment using state of the art facilities.
- To provide adequate practical training to meet the requirement of the Electronics & communication industry.
- To train the students to take up leadership roles in their career or to pursue higher education and research.

PROGRAMME EDUCATIONAL OBJECTIVES AND OUTCOMES
M.Tech. VLSI and Embedded Systems

PROGRAMME EDUCATIONAL OBJECTIVES

- To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design.
- To provide technical skills in software and hardware tools related to the design and implementation of integrated Circuits, System on Chip for real time applications.
- To provide scope for Applied Research and innovation in the various fields of VLSI and Embedded Systems, and enabling the students to work in the emerging areas.
- To enhance communication and soft skills of students to make them work effectively as a team.

PROGRAMME OUTCOMES

On completion of the program, the graduates will

- Be able to analyze, design and implement Analog, Digital and Mixed Signal Circuits and real time embedded systems.
- Have in-depth knowledge and capability to use industry standard tools in the design and implementation of VLSI and real time Embedded Systems.
- Be able to undertake research projects in related domains of VLSI and Embedded systems.
- Possess the capability to communicate effectively and work as a team in the professional career.

B.S.ABDUR RAHMAN
UNIVERSITY
B.S. ABDUR RAHMAN INSTITUTE OF SCIENCE & TECHNOLOGY
(Estd.u/s 3 of the UGC Act, 1956)
(FORMERLY B.S.ABDUR RAHMAN CRESCENT ENGINEERING COLLEGE)
Seethakathi Estate, G.S.T. Road, Vandalur, Chennai - 600 048.

REGULATIONS 2013
FOR
M.TECH. DEGREE PROGRAMMES
(WITH AMENDMENTS INCORPORATED TILL JUNE 2015)

B.S. ABDUR RAHMAN UNIVERSITY, CHENNAI 48.
REGULATIONS -2013 FOR M.TECH / MCA / M.Sc. DEGREE PROGRAMMES

(With amendments incorporated till June 2015)

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires

i) **"Programme"** means Post Graduate Degree Programme (M.Tech./ MCA / M.Sc.)

ii) **"Course"** means a theory or practical subject that is normally studied in a semester, like Applied Mathematics, Structural Dynamics, Computer Aided Design, etc.

iii) **"University"** means B.S.Abdur Rahman University, Chennai, 600048.

iv) **"Institution"** unless otherwise specifically mentioned as an autonomous or off campus institution means B.S.Abdur Rahman University.

v) **"Academic Council"** means the Academic Council of this University.

vi) **"Dean (Academic Affairs)"** means Dean (Academic Affairs) of B.S.Abdur Rahman University.

vii) **"Dean (Student Affairs)"** means Dean(Student Affairs) of B.S.Abdur Rahman University.

viii) **"Controller of Examinations"** means the Controller of Examinations of B.S.Abdur Rahman University who is responsible for conduct of examinations and declaration of results.

2.0 PROGRAMMES OFFERED, MODE OF STUDY AND ADMISSION REQUIREMENTS

2.1 P.G. Programmes Offered

The various P.G. Programmes and their modes of study are as follows:

Degree	Mode of Study
M.Tech.	Full Time
M.Tech.	Part Time – Day / Evening
M.C.A.	Full Time
M. Sc.	Full Time
M. Sc.	Full Time

2.2 MODES OF STUDY

2.2.1 Full-time

Students admitted under "Full-Time" shall be available in the Institution during the complete working hours for curricular, co-curricular and extra-curricular activities assigned to them.

2.2.2 A full time student, who has completed all non-project courses desiring to do the Projectwork in part-time mode for valid reasons, shall apply to the Dean (Academic Affairs) through the Head of the Department, if the student satisfies the clause 2.3.4 of this Regulation. Permission may be granted based on merits of the case. Such conversion is not permitted in the middle of a semester.

2.2.3 Part time - Day time

In this mode of study, the students are required to attend classes for the courses registered along with full time students.

2.2.4 Part time - Evening

In this mode of study, the students are required to attend normally classes in the evening and on Saturdays, if necessary.

2.2.5 A part time student is not permitted to convert to full time mode of study.

2.3 ADMISSION REQUIREMENTS

2.3.1 Students for admission to the first semester of the Master's Degree Programme shall be required to have passed the appropriate degree examination of this University as specified in the Table shown for eligible entry qualifications for admission to P.G. programmes or any other degree examination of any University or authority accepted by this University as equivalent thereto.

2.3.2 Eligibility conditions for admission such as class obtained, number of attempts in the qualifying examination and physical fitness will be as prescribed by this Institution from time to time.

2.3.3 All part-time students should satisfy other conditions regarding experience, sponsorship etc., which may be prescribed by this Institution from time to time.

2.3.4 A student eligible for admission to M.Tech. Part Time / Day Time programme shall have his/her permanent place of work within a distance of 65km from the campus of this Institution.

2.3.5 Student eligible for admission to M.C.A under lateral entry scheme shall be required to have passed three year degree in B.Sc (Computer Science) / B.C.A / B.Sc (Information Technology)

3.0 DURATION AND STRUCTURE OF THE P.G. PROGRAMME

3.1 The minimum and maximum period for completion of the P.G. Programmes are given below:

Programme	Min.No.of Semesters	Max.No.of Semesters
M.Tech. (Full Time)	4	8
M.Tech.(Part Time)	6	12
M.C.A. (Full Time)	6	12
M.C.A. (Full Time) – (Lateral Entry)	4	8
M.Sc. (Full Time)	4	8

3.2 The PG. programmes consist of the following components as prescribed in the respective curriculum

i. Core courses
ii. Elective courses
iii. Project work / thesis / dissertation
iv. Laboratory Courses
v. Case studies
vi. Seminars
vii. Industrial Internship

3.3 The curriculum and syllabi of all PG. programmes shall be approved by the Academic Council of this University.

3.4 The minimum number of credits to be earned for the successful completion of the programme shall be specified in the curriculum of the respective specialization of the P.G. programme.

3.5 Each academic semester shall normally comprise of 80 working days. Semester-end examinations will follow immediately after the last working day.

ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO P.G. PROGRAMMES

Sl. No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
01.	Civil Engineering	M.Tech. (Structural Engineering)	B.E / B.Tech. (Civil Engineering) / (Structural Engineering)
		M.Tech. (Construction Engineering and Project Management)	
02.	Mechanical Engineering	M.Tech. (Manufacturing Engineering)	B.E. / B.Tech. (Mechanical / Auto / Manufacturing / Production / Industrial / Mechatronics / Metallurgy / Aerospace /Aeronautical / Material Science / Marine Engineering)
		M.Tech. CAD / CAM	
03.	Polymer Engineering	M.Tech. (Polymer Technology)	B.E./ B.Tech. degree Mech./Production/ Polymer Science or Engg or Tech / Rubber Tech / M.Sc (Polymer Sc./ Chemistry Appl. Chemistry)
04.	Electrical and Electronics Engineering	M.Tech. (Power Systems Engg)	B.E / B.Tech (EEE / ECE / E&I / I&C / Electronics / Instrumentation)
		M.Tech. (Power Electronics & Drives)	
05.	Electronics and Communication Engineering	M.Tech. (Communication Systems)	B.E / B.Tech (EEE/ ECE / E&I / I&C / Electronics / Instrumentation)
		M.Tech.(VLSI and Embedded Systems)	B.E./ B.Tech. in ECE / Electronics / EIE / ICE / EEE
		M.Tech.(Signal Processing)	
06.	ECE Department jointly with Physics Dept	M.Tech. (Optoelectronics and Laser Technology)	B.E./B.Tech. (ECE / EEE / Electronics / EIE / ICE) M.Sc (Physics / Materials Science / Electronics / Photonics)
07.	Electronics and Instrumentation Engineering	M.Tech. (Electronics and Instrumentation Engineering)	B.E./ B.Tech. (EIE/ICE/Electronics/ECE/ EEE)
08.	Computer Science and Engineering	M.Tech. (Computer Science and Engineering)	B.E. /B.Tech. (CSE/IT/ECE/EEE/EIE/ICE/ Electronics) MCA
		M.Tech. (Software Engineering)	B.E. / B.Tech. (CSE / IT) MCA
		M.Tech (Network Security)	B.E. /B.Tech. (CSE/IT/ECE/EEE/EIE/ICE/ Electronics) MCA
		M.Tech (Computer and Predictive Analytics)	
		M.Tech. (Computer Science and Engineering with specialization in Big Data Analytics)	
09	Information Technology	M.Tech. (Information Technology)	B.E /B.Tech. (IT/CSE/ECE/EEE/EIE/ICE/ Electronics) MCA
		M.Tech. (Information Security & Digital Forensics)	

ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO P.G. PROGRAMMES

Sl. No.	Name of the Department	P.G. Programmes offered	Qualifications for admission
10	Computer Applications	M.C.A.	Bachelor Degree in any discipline with Mathematics as one of the subjects (or) Mathematics at +2 level
		M.C.A. (Full Time) – (Lateral Entry)	B.Sc Computer Science / B.Sc Information Technology / B.C.A
		M.Tech. (Systems Engineering and Operations Research)	BE / B.Tech. (Any Branch) or M.Sc., (Maths / Physics / Statistics / CS / IT / SE) or M.C.A.
		M.Tech. (Data & Storage Management)	
11	Mathematics	M.Sc. (Actuarial Science)	Any Degree with Mathematics / Statistics as one of the Subjects of Study.
		M.Sc. Mathematics	B.Sc. (Mathematics)
12	Physics	M.Sc.(Physics)	B.Sc.(Physics / Applied Science / Electronics / Electronics Science / Electronics & Instrumentation)
		M.Sc. (Material Science)	
13	Chemistry	M.Sc.(Chemistry)	B.Sc (Chemistry) of B.Sc. (Applied Science)
14	Life Sciences	M.Sc. Molecular Biology & Biochemistry	B.Sc. in any branch of Life Sciences
		M.Sc. Genetics	B.Sc. in any branch of Life Sciences
		M.Sc. Biotechnology	B.Sc. in any branch of Life Sciences
		M.Sc. Microbiology	B.Sc. in any branch of Life Sciences
		M.Sc. Bioscience	B.Sc. in any branch of Life Sciences
		M.Tech. Biotechnology	B.Tech. (Biotechnology / Chemical Engineering) / M.Sc. in any branch of Life Sciences

3.6 The curriculum of PG programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below:

Programme	Minimum prescribed credit range
M.Tech.	75 to 85
M.C.A.	120 to 130
M.Sc.	75 to 85

3.7 Credits will be assigned to the courses for all P.G. programmes as given below:

* One credit for one lecture period per week
* One credit for one tutorial period per week
* One credit each for seminar/practical session/project of two or three periods per week
* One credit for two weeks of industrial internship.

3.8 The number of credits registered by a student in non-project semester and project semester should be within the range specified below:

P.G. Programme	Non-project Semester	Project semester
M.Tech. (Full Time)	15 to 29	12 to 20
M.Tech. (Part Time)	6 to 18	12 to 16
M.C.A. (Full Time)	15 to 29	12 to 20
M.Sc. (Full Time)	15 to 25	12 to 20

3.9 The electives from the curriculum are to be chosen with the approval of the Head of the Department.

3.10 A student may be permitted by the Head of the Department to choose electives offered from other PG programmes either within the Department or from other Departments up to a maximum of three courses during the period of his/her study, provided the Heads of the Departments offering such courses also agree.

3.11 To help the students to take up special research areas in their project work and to enable the department to introduce courses in latest/emerging areas in the curriculum, "Special Electives" may be offered. A student may be permitted to register for a "Special Elective" up to a maximum of three credits during the period of his/her study, provided the syllabus of this course is recommended by the Head of the Department and approved by the Chairman, Academic Council before the commencement of the semester, in which the special elective course is offered. Subsequently, such course shall be ratified by the Board of Studies and Academic Council.

3.12 The medium of instruction, examination, seminar and project/thesis/ dissertation reports will be English.

3.13 Industrial internship, if specified in the curriculum shall be of not less than two weeks duration and shall be organized by the Head of the Department.

3.14 PROJECT WORK/THESIS/DISSERTATION

3.14.1 Project work / Thesis / Dissertation shall be carried out under the supervision of a qualified teacher in the concerned Department.

3.14.2 A student may however, in certain cases, be permitted to work for the project in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from the organization and the student shall be instructed to meet the faculty periodically and to attend the review committee meetings for evaluating the progress.

3.14.3 Project work / Thesis / Dissertation (Phase - II in the case of M.Tech.) shall be pursued for a minimum of 16 weeks during the final semester, following the preliminary work carried out in Phase-1 during the previous semester.

3.14.4 The Project Report/Thesis / Dissertation report / Drawings prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

3.14.5 The deadline for submission of final Project Report / Thesis / Dissertation is within 30 calendar days from the last working day of the semester in which Project / Thesis / Dissertation is done.

3.14.6 If a student fails to submit the Project Report / Thesis / Dissertation on or before the specified deadline he / she is deemed to have not completed the Project Work / Thesis / dissertation and shall re-register the same in a subsequent semester.

3.14.7 A student who has acquired the minimum number of total credits prescribed in the Curriculum for the award of Masters Degree will not be permitted to enroll for more courses to improve his/her cumulative grade point average (CGPA).

4.0 CLASS ADVISOR AND FACULTY ADVISOR

4.1 CLASS ADVISOR

A faculty member will be nominated by the HOD as Class Advisor for the whole class.

He/she is responsible for maintaining the academic, curricular and co-curricular records of all students throughout their period of study.

4.2 FACULTY ADVISOR

To help the students in planning their courses of study and for general counseling on the academic programme, the Head of the Department of the students will attach a certain number of students to a faculty member of the department who shall function as Faculty Advisor for the students throughout their period of study. Such Faculty Advisor shall offer advice to the students on academic and personal matters, and guide the students in taking up courses for registration and enrolment every semester.

5.0 CLASS COMMITTEE

5.1 Every class of the PG Programme will have a Class Committee constituted by the Head of the Department as follows:

i. Teachers of all courses of the programme

ii. One senior faculty preferably not offering courses for the class, as Chairperson.

iii. Minimum two students of the class, nominated by the Head of the Department.

iv. Class Advisor / Faculty Advisor of the class - Ex-Officio Member

v. Professor in-charge of the PG Programme - Ex-Officio Member.

5.2 The Class Committee shall be constituted by the respective Head of the Department of the students.

5.3 The basic responsibilities of the Class Committee are to review periodically the progress of the classes to discuss problems concerning curriculum and syllabi and the conduct of classes. The type of assessment for the course will be decided by the teacher in consultation with the Class Committee and will be announced to the students at the beginning of the semester. Each Class Committee will communicate its recommendations to the Head of the Department and Dean (Academic Affairs). The class committee, without the student members, will also be responsible for finalization of the semester results and award of grades.

5.4 The Class Committee is required to meet at least thrice in a semester, first within a week of the commencement of the semester, second, after the first assessment and the third, after the semester-end examination to finalize the grades.

6.0 COURSE COMMITTEE

Each common theory course offered to more than one group of students shall have a "Course Committee" comprising all the teachers teaching the common course with one of them nominated as Course coordinator. The nomination of the Course coordinator shall be made by the Head of the Department / Dean (Academic Affairs) depending upon whether all the teachers teaching the common course belong to a single department or to several departments. The Course Committee shall meet as often as possible and ensure uniform evaluation of the tests and arrive at a common scheme of evaluation for the tests. Wherever it is feasible, the Course Committee may also prepare a common question paper for the test(s).

7.0 REGISTRATION AND ENROLMENT

7.1 For the first semester every student has to register and enroll for all the courses.

7.2 For the subsequent semesters registration for the courses will be done by the student during a specified week before the semester-end examination of the previous semester. The curriculum gives details of the core and elective courses, project and seminar to be taken in different semester with the number of credits. The student should consult his/her Faculty Adviser for the choice of courses. The Registration form shall be filled in and signed by the student and the Faculty Adviser.

7.3 From the second semester onwards all students shall pay the prescribed fees and enroll on a specified day at the beginning of a semester.

7.4 A student will become eligible for enrolment only if he/she satisfies clause 9 and in addition he/she is not debarred from enrolment by a disciplinary action of the Institution. At the time of enrolment a student can drop a course registered earlier and also substitute it by another course for valid reasons with the consent of the Faculty Adviser. Late enrolment will be permitted on payment of a prescribed fine up to two weeks from the date of commencement of the semester.

7.5 Withdrawal from a course registered is permitted up to one week from the date of the completion of the first assessment test.

7.6 Change of a course within a period of 15 days from the commencement of the course, with the approval of Dean (Academic Affairs), on the recommendation of the HOD, is permitted.

7.7 Courses withdrawn will have to be taken when they are offered next if they belong to the list of core courses.

7.8 A student should have registered for all preceding semesters before registering for a particular semester.

8.0 TEMPORARY BREAK OF STUDY FROM THE PROGRAMME

A student may be permitted by the Dean (Academic Affairs) to avail temporary break of study from the programme up to a maximum of two semesters for reasons of ill health or other valid grounds. Such student has to rejoin only in the same semester from where he left. However the total duration for completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1).

9.0 MINIMUM REQUIREMENTS TO REGISTER FOR PROJECT / THESIS / DISSERTATION

9.1 A student is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	**Minimum No. of credits to be earned to enroll for project semester**
M.Tech. (Full time)	18 (III semester)
M.Tech. (Part time)	18 (V semester)
M.C.A. (Full time)	45 (V semester)
M.C.A. (Full time) – (Lateral Entry)	22 (V semester)
M.Sc.(Full time)	30 (IV semester) if project is in IV semester 18 (III semester) if project is in III semester

9.2 If the student has not earned minimum number of credits specified, he/she has to earn the required credits, at least to the extent of minimum credits specified in clause 9.1 and then register for the project semester.

10.0 DISCIPLINE

10.1 Every student is required to observe discipline and decorous behavior both inside and outside the campus and not to indulge in any activity, which will tend to bring down the prestige of the Institution.

10.2 Any act of indiscipline of a student reported to the Head of the Institution will be referred to a Discipline and Welfare Committee for taking appropriate action.

10.3 Every student should have been certified by the HOD that his / her conduct and discipline have been satisfactory.

11.0 ATTENDANCE

11.1 Attendance rules for all Full Time Programme and Part time - day Time Programmes are given in the following sub-clause.

11.2 Ideally every student is expected to attend all classes and earn 100% attendance in the contact periods of every course, subject to a maximum relaxation of 25% for genuine reasons like on medical grounds, representing the University in approved events etc., to become eligible to appear for the semester-end examination in that course, failing which the student shall be awarded "I" grade in that course. If the course is a core course, the student should register for and repeat the course when it is offered next. If the course is an elective, either he/she can register and repeat the same elective or can register for a new elective.

11.3 The students who have not attended a single hour in all courses in a semester and awarded 'I' grade are not permitted to write the examination and also not permitted move to next higher semester. Such students should repeat all the courses of the semester in the next Academic year.

12.0 SUMMER TERM COURSES

12.1 Summer term courses may be offered by a department on the recommendation of the Departmental Consultative Committee and approved by the Dean (Academic Affairs). No student should register for more than three courses during a summer term.

12.2 Summer term courses will be announced by the Head of the department at the end of the even semester before the commencement of the end semester examinations. A student will have to register within the time stipulated in the announcement. A student has to pay the fees as stipulated in the announcement.

12.3 The number of contact hours and the assessment procedure for any course during summer term will be the same as those during regular semesters.

Students with U grades will have the option either to write semester end arrears exam or to redo the courses during summer / regular semesters, if they wish to improve their continuous assessment marks subject to the approval of the Head of the department.

12.4 Withdrawal from a summer term course is not permitted. No substitute examination will be conducted for the summer term courses.

13.0 ASSESSMENTS AND EXAMINATIONS

13.1 The following rule shall apply to the full-time and part-time PG programmes (M.Tech./ M.C.A. / M.Sc.)

For lecture-based courses, normally a minimum of two assessments will be made during the semester. The assessments may be combination of tests and assignments. The assessment procedure as decided in the Class Committee will be announced to the students right from the beginning of the semester by the course teacher.

13.2 There shall be one examination of three hours duration, at the end of the semester, in each lecture based course.

13.3 The evaluation of the Project work will be based on the project report and a Viva-Voce Examination by a team consisting of the supervisor concerned, an Internal Examiner and External Examiner to be appointed by the Controller of Examinations.

13.4 At the end of industrial internship, the student shall submit a certificate from the organization and also a brief report. The evaluation will be made based on this report and a Viva-Voce Examination, conducted internally by a Departmental Committee constituted by the Head of the Department.

14.0 WEIGHTAGES

14.1 The following shall be the weightages for different courses:

(i) Lecture based course

Two continuous assessments	- 50%
Semester-end examination	- 50%

(ii) Laboratory based courses

Laboratory work assessment	- 75%
Semester-end examination	- 25%

(iii) Project work

Periodic reviews	- 50%
Evaluation of Project Report by External Examiner	- 20%
Viva-Voce Examination	- 30%

14.2 Appearing for semester end examination for each course (Theory and Practical) is mandatory and a student should secure a minimum of 40% marks in semester end examination for the successful completion of the course.

14.3 The markings for all tests, tutorial, assignments (if any), laboratory work and examinations will be on absolute basis. The final percentage of marks is calculated in each course as per the weightages given in clause 13.1.

15.0 SUBSTITUTE EXAMINATION

15.1 A student who has missed for genuine reasons any one of the three assessments including semester-end examination of a course may be permitted to write a substitute examination. However, permission to take up a substitute examination will be given under exceptional circumstances, such as accident or admissions to a hospital due to illness, etc.

15.2 A student who misses any assessment in a course shall apply in a prescribed form to the Dean (Academic Affairs) through the Head of the department within a week from the date of missed assessment. However the substitute tests and examination for a course will be conducted within two weeks after the last day of the semester-end examinations.

16.0 COURSEWISE GRADING OF STUDENTS AND LETTER GRADES

16.1 Based on the semester performance, each student is awarded a final letter grade at the end of the semester in each course. The letter grades and the corresponding grade points are as follows, but grading has to be relative grading

Letter grade	Grade points
S	10
A	9
B	8
C	7
D	6
E	5
U	0
W	-
I	-
AB	-

Flexible range grading system will be adopted

“W” denotes withdrawal from the course.

"I" denotes inadequate attendance and hence prevention from semester-end examination

"U" denotes unsuccessful performance in a course.

“AB” denotes absent for the semester end examination

16.2 A student is considered to have completed a course successfully if he / she secure five grade points or higher. A letter grade ‘U’ in any course implies unsuccessful performance in that course.

16.3 A course successfully completed cannot be repeated for any reason.

17.0 AWARD OF LETTER GRADE

17.1 A final meeting of the Class Committee without the student member(s) will be convened within ten days after the last day of the semester end examination. The letter grades to be awarded to the students for different courses will be finalized at the meeting.

17.2 After finalization of the grades at the class committee meeting the Chairman will forward the results to the Controller of Examinations, with copies to Head of the Department and Dean (Academic Affairs).

18.0 DECLARATION OF RESULTS

18.1 After finalization by the Class Committee as per clause 16.1 the Letter grades awarded to the students in the each course shall be announced on the departmental notice board after duly approved by the Controller of Examinations.

18.2 In case any student feels aggrieved about the results, he/she can apply for revaluation after paying the prescribed fee for the purpose, within one week from the announcement of results.

A committee will be constituted by the concerned Head of the Department comprising of the Chairperson of the concerned Class Committee (Convener), the teacher concerned and a teacher of the department who is knowledgeable in the concerned course. If the Committee finds that the case is genuine, it may jointly revalue the answer script and forward the revised marks to the Controller of Examinations with full justification for the revision, if any.

18.3 The “U” and “AB” grade once awarded stays in the grade sheet of the students and is not deleted when he/she completes the course successfully later. The grade acquired by the student later will be indicated in the grade sheet of the appropriate semester.

19.0 COURSE REPETITION AND ARREARS EXAMINATION

19.1 A student should register to re-do a core course wherein "I" or "W" grade is awarded. If the student is awarded "I" or "W" grade in an elective course either the same elective course may be repeated or a new elective course may be taken.

19.2 A student who is awarded "U" or "AB" grade in a course shall write the semester-end examination as arrear examination, at the end of the next semester, along with the regular examinations of next semester courses.

19.3 A student who is awarded "U" or "AB" grade in a course will have the option of either to write semester end arrear examination at the end of the subsequent semesters, or to redo the course whenever the course is offered. Marks earned during the redo period in the continuous assessment for the course, will be used for grading along with the marks earned in the end-semester (re-do) examination.

19.4 If any student obtained "U" or "AB" grade, the marks earned during the redo period for the continuous assessment for that course will be considered for further appearance as arrears.

19.5 If a student with "U" or "AB" grade prefers to redo any particular course fails to earn the minimum 75% attendance while doing that course, then he/she will not be permitted to write the semester end examination and his / her earlier 'U' grade and continuous assessment marks shall continue.

20.0 GRADE SHEET

20.1 The grade sheet issued at the end of the semester to each student will contain the following:

(i) the credits for each course registered for that semester.

(ii) the performance in each course by the letter grade obtained.

(iii) the total credits earned in that semester.

(iv) the Grade Point Average (GPA) of all the courses registered for that semester and the Cumulative Grade Point Average (CGPA) of all the courses taken up to that semester.

20.2 The GPA will be calculated according to the formula

$$GPA = \frac{\sum_{i=1}^{n}(C_i)(GPi)}{\sum_{i=1}^{n} C_i} \qquad Where\ \ n = number\ of\ courses$$

where Ci is the number of credits assigned for i^{th} course

GP_i - Grade point obtained in the i^{th} course

For the cumulative grade point average (CGPA) a similar formula is used except that the sum is over all the courses taken in all the semesters completed up to the point of time.

'I' and 'W' grades will be excluded for GPA calculations.

'U', 'AB' 'I' and 'W' grades will be excluded for CGPA calculations.

20.3 Classification of the award of degree will be as follows:

CGPA	Classification
8.50 and above, having completed all courses in first appearance	First class with Distinction
6.50 and above, having completed within a period of 2 semesters beyond the programme period	First Class
All others	Second Class

However, to be eligible for First Class with Distinction, a student should not have obtained U or I grade in any course during his/her study and should have completed the PG Programme within a minimum period covered by the minimum duration (clause 3.1) plus authorized break of study, if any (clause 8). To be eligible for First Class, a student should have passed the examination in all courses within the specified minimum number of semesters reckoned from his/her commencement of study plus two semesters. For this purpose, the authorized break of study will not be counted. The students who do not satisfy the above two conditions will be classified as second class. For the purpose of classification, the CGPA will be rounded to two decimal places. For the purpose of comparison of performance of students and ranking, CGPA will be considered up to three decimal places.

21.0 ELIGIBILITY FOR THE AWARD OF THE MASTERS DEGREE

21.1 A student shall be declared to be eligible for the award of the Masters Degree, if he/she has:

i) successfully acquired the required credits as specified in the Curriculum corresponding to his/her programme within the stipulated time,

ii) no disciplinary action is pending against him/her.

21.2 The award of the degree must be approved by the University.

22.0 POWER TO MODIFY

Notwithstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

CURRICULUM & SYLLABI FOR M.TECH.(VLSI AND EMBEDDED SYSTEMS) (FOUR SEMESTERS / FULL TIME)

CURRICULUM

SEMESTER I

Sl. No	Course Code	Course Title	L	T	P	C
1.	MAB6186	Applied Mathematics for Electronics Engineers	3	1	0	4
2.	ECB6121	Advanced Digital System Design	3	0	0	3
3.	ECB6122	VLSI Design Methodologies	3	0	0	3
4.	ECB6123	Design of Embedded Systems	3	0	0	3
5.	ECB6101	Research Methodology Electronics Engineers	3	0	0	3
6.		Elective I	3	0	0	3
7.	ECB6124	VLSI Physical Design Lab	0	0	3	1
8.	ECB6125	Embedded System lab	0	0	3	1
9.	ECB6126	Seminar	0	0	2	1
						22

SEMESTER II

Sl. No	Course Code	Course Title	L	T	P	C
1.	ECB6231	ASIC Design	3	0	0	3
2.	ECB6232	Analog Integrated Circuit Design	3	0	0	3
3.	ECB6233	Real Time Operating Systems	3	0	0	3
4.	ECB6234	Advanced Embedded Systems	3	0	0	3
5.		Elective II	3	0	0	3
6.		Elective III	3	0	0	3
7.	ECB6235	Analog IC Design Lab	0	0	3	1
8.	ECB6236	Design/Fabrication Project	0	0	3	1
						20

SEMESTER III

Sl. No	Course Code	Course Title	L	T	P	C
1.		Elective IV	3	0	0	3
2.		Elective V	3	0	0	3
3.		Elective VI	3	0	0	3
4.	ECB7102	Project Management	3	0	0	3
5.	ECB7121	Project Work - Phase I	0	0	12	6*
						12

SEMESTER IV

Sl. No	Course Code	Course Title	L	T	P	C
1.	ECB7121	Project Work - Phase II	0	0	36	18*
						18 + 6 = 24

* Credits for Project Work Phase I to be accounted along with Project Work Phase II in IV Semester

TOTAL CREDITS : 78

LIST OF ELECTIVES

Sl. No	Course Code	Course
1.	ECBY26	Low Power VLSI Design
2.	ECBY27	RF Integrated Circuits Design
3.	ECBY28	Advanced Microprocessors & Microcontrollers
4.	ECBY29	CAD for VLSI Circuits
5.	ECBY30	Reconfigurable Computing
6.	ECBY31	Testing of VLSI Circuits
7.	ECBY32	CMOS Mixed Signal Circuit Design
8.	ECBY33	Embedded Networking
9.	ECBY34	RISC Processor Architecture and Programming
10.	ECBY35	Distributed Embedded Computing
11.	ECBY36	Design of Semiconductor Memories
12.	ECBY37	Control Area Network
13.	ECBY38	Introduction To MEMS System Design
14.	ECBY39	Applications of MEMS technology
15.	ECBY40	Hardware-software co-design
16.	ECBY41	System Verilog
17.	ECBY42	Soc design and verification
18.	ECBY43	Signal integrity for high speed design
19.	ECBY44	Optimization techniques and their applications in VLSI design
20.	ECBY45	VLSI Signal Processing
21.	ECBY46	Evolutionary Computation
22.	ECBY01	Digital Image Processing
23.	SSBY01	Society, Technology & Sustainability

SEMESTER I

MAB 6186 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS **L T P C 3 1 0 4**

OBJECTIVES:

- Familiarizing students with numerical techniques in solving system of equations and Eigenvalue problem.
- Exposing students, the significance of special functions and their properties.
- Introducing the concepts of random variables and queueing models.

MODULE I SYSTEM OF EQUATIONS AND EIGEN VALUE PROBLEM 7

System of Equations – Solution by Gauss Elimination, Gauss-Jordon and LU decomposition method – Jacobi, Gauss-Seidal iteration method – Eigen values of a matrix by Jacobi and Power methods.

MODULE II WAVE EQUATION 8

Solution of initial and boundary value problems-Characteristics-D'Alembert's Solution –Significance of characteristic curves - Laplace transform solution for displacement in a long string – a long string under its weight-Longitudinal vibration of a elastic bar with prescribed force on one end - free vibrations of a string.

MODULE III SPECIAL FUNCTIONS 8

Bessel's equation - Bessel Functions - Legendre's equation - Legendre polynomials -Rodrigue's formula - Recurrence relations - generating functions and orthogonal property of Bessel function and Legendre Polynomials.

MODULE IV RANDOM VARIABLES 7

One dimensional Random Variables - Moments and Moment Generating Function - Binomial, Poisson, Geometrical, Uniform, Exponential, Normal and Weibull distributions.

MODULE V TWO DIMENSIONAL RANDOM VARIABLES 7

Two dimensional Random Variables - Marginal and Conditional distribution - Covariance and Correlation coefficient - Functions of one dimensional and two dimensional Random Variables.

MODULE VI QUEUEING THEORY **8**

Poisson Process – Markovian Queues – Single and Multi-server Models – Little's formula – Machine Interference Model – Steady State analysis – Self Service Queue – Network Optimal Path.

Total Hours : 60

REFERENCES:

1. Jain M.K., Iyengar .S.R.K: & Jain.R.K, "Numerical Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publishers, 2003.
2. Grewal B.S, "Higher Engineering Mathematics", Khanna Publishers, 2005.
3. Taha H.A, "Operations Research – An Introduction", Prentice Hall of India, 2001.
4. Sankara Rao K., "Introduction to Partial Differential Equation", Prentice Hall of India, 1997.
5. Gross.D & Harris.C.M, "Fundamentals of Queuing Theory", John Wiley & Sons, 1985.
6. Robert V. Hogg, Joseph W. McKean, Allen Thornton Craig "Introduction to Mathematical Statistics", Pearson Education, 2012.
7. V. K. Rohatgi, A. K. Md. Ehsanes Saleh, "An Introduction to Probability and Statistics", John Wiley & Sons, 2001.

OUTCOMES:

At the end of the course students will be able to

- solve large system of linear equations and eigen value problem of a matrix numerically.
- use special functions and Laplace transform as a tool for solving engineering problems.
- solve wave equation using several techniques.

ECB6121 ADVANCED DIGITAL SYSTEM DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To provide knowledge to design sequential and asynchronous sequential circuit.
- To introduce programmable logic devices and its application to circuit design,
- To introduce the concepts involved in designing fault free circuits.

MODULE I SEQUENTIAL CIRCUIT DESIGN 11

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modelling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier- Verilog design of Sequential circuits

MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 11

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Designing vending Machine Controller – Mixed Operating Mode Asynchronous Circuits- Verilog design of Asynchronous circuits

MODULE III NEW GENERATION PROGRAMMABLE LOGIC DEVICES 14

ROM- Internal ROM structure – Implementation of Boolean functions using ROM- Design of Sequential circuits using ROM, PROM – Realization State machine using PLD, PAL, PLA, Programmable Gate Arrays, Programmable Logic sequencer, Field Programmable Gate Array Families. Verilog design of programmable logic devices

MODULE IV FAULT DIAGONOSIS AND TESTING 9

Fault detection and location, gate sensitivity, path sensitization, undetectable faults, bridging fault, two level circuit fault detection, Boolean difference, compact testing technique, scan path testing, design for testability.

Total Hours :45

REFERENCES:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2002.
2. Stephen Brown and Zvonk Vranesic, “Fundamentals of Digital Logic with Verilog Design”, Tata McGraw Hill, 2002.
3. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
4. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.
5. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
6. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.
7. Digital Logic Design, IV edition, Brian Holdsworth, Clive Woods, Elesevier, 2008.
8. Michael D Ciletti, “Advanced Digital Design with the Verilog HDL”, PHI, 2008.

OUTCOMES:

At the end of the course the student

- will be able to design synchronous and asynchronous sequential circuits.
- will be able to use programmable logic devices for designing of circuits
- will perform fault diagnosis and testing in digital circuit.

ECB6122 VLSI DESIGN METHODOLOGIES L T P C

3 0 0 3

OBJECTIVES:

This course will cover

- CMOS circuit characteristics and their performance.
- Design methodology and tools.
- Design for testability.
- Major building blocks (adders, multipliers, RAMs, and ROMs)
- Clocks and power distribution networks.
- I/O pads and packaging .

MODULE I CMOS CIRCUITS 9

MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter - The Transmission Gate, The Tri State Inverter, Bipolar Devices.

MODULE II CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, Reliability.

MODULE III CMOS CIRCUIT AND LOGIC DESIGN 8

CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design

MODULE IV SYSTEMS DESIGN AND DESIGN METHOD 9

Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing -Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.

MODULE V CMOS SUB SYSTEM DESIGN **10**

Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Total Hours : 45

REFERENCES:

1. Neil. H.E. Weste and K. Eshragian, “Principles of CMOS VLSI Design”. 2nd Edition, Addison-Wesley, 2000.
2. Douglas a. Pucknell and K. Eshragian., “Basic VLSI Design” 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., “CMOS Circuit Design”, 3rd Indian reprint, PHI, 2000.
4. Kang & Leblebigi “CMOS Digital IC Circuit Analysis & Design”- McGraw Hill, 2003
5. Jacob Backer, Harry W. Li and David E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Prentice Hall of India, 1998.
6. William M. Penny, Lillian Lau, “MOS Integrated Circuits- Theory, Fabrication, Design and System Applications of MOS LSI”, Van Nostrand Reihold Company.

OUTCOMES:

On successful completion of this course, students will be able to

- know basics of VLSI design fundamentals
- know various mathematical approaches for designing
- study the performance of CMOS circuits
- to design complex VLSI circuits
- to design low power systems
- analyze and synthesize the building blocks of CMOS subsystem.

ECB6123 DESIGN OF EMBEDDED SYSTEMS L T P C

3 0 0 3

OBJECTIVES:

To impart knowledge on

- Embedded product design covering various dimensions of product development, Quality principles, Project Management and discussion with suitable case study.
- Co-synthesis of Embedded hardware and software.

MODULE I EMBEDDED DESIGN LIFE CYCLE 9

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – RTOS availability – Tool chain availability – Other issues in selection processes.

MODULE II PARTITIONING DECISION 9

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System start-up – Hardware manipulation – memory mapped access – speed and code density.

MODULE III INTERRUPT SERVICE ROUTINES 9

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyzer – Caches – Computer optimization – Statistical profiling.

MODULE IV IN-CIRCUIT EMULATORS 9

Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

MODULE V TESTING 9

Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

Total Hours : 45

REFERENCES:

1. Arnold S. Berger – “Embedded System Design: An introduction to processor, tools and techniques”, CMP books, USA, 2002.
2. Sriram Iyer, “Embedded Real time System Programming”, Tata McGraw Hill, 2003.
3. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.
4. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.

OUTCOMES:

After successful completion of the course, the students shall

- understand the quality principles and tools in product development process, right from identifying customer requirements and translating them into product specifications and realization of the product specifications through electronics, mechanical and industrial design, product engineering and meeting the cost and development time constraints through better project management.
- illustrate the differences between various types of system software (real-time, information systems, fault tolerant).
- understand the division of hardware/software in embedded systems.

ECB6101	RESEARCH METHODOLOGY FOR ELECTRONICS ENGINEERS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce students to a number of perspectives on research and to broaden their conceptions of what research involves.
- To learn about research, design, information retrieval, problem formulation, use of statistical techniques, evaluation and writing of research reports, papers and ethics in research.

MODULE I RESEARCH PROBLEM FORMULATION 7

Research - objectives - types, Research process, solving engineering problems-Identification of research topic - Formulation of research problem, literature survey and review.

MODULE II RESEARCH DESIGN 8

Research design - meaning and need - basic concepts - Different research designs, Experimental design - principle - important experimental designs, Design of experimental setup, Mathematical modeling - Simulation, validation and experimentation - Dimensional analysis - similitude.

MODULE III USE OF STATISTICAL TOOLS IN RESEARCH 12

Importance of statistics in research - Concept of probability - Popular distributions - Sample design. Hypothesis testing, ANOVA, Design of experiments - Factorial designs - Orthogonal arrays, Multivariate analysis - correlation and regression, Curve fitting.

MODULE IV ANALYSIS AND INTERPRETATION OF DATA 10

Research Data analysis - Interpretation of results- Correlation with scientific facts - repeatability and reproducibility of results - Accuracy and precision - limitations, Use of optimization techniques - Traditional methods – evolutionary optimization techniques.

MODULE V THE RESEARCH REPORT 8

Purpose of written report - Audience - Synopsis writing - preparing papers for International Journals-thesis writing - Organization of contents - style of writing-

graphs and charts - Referencing, Oral presentation and defence - Ethics in research - Patenting, IPR.

Total Hours : 45

REFERENCES:

1. Ganesan.R., ”Research methodology for Engineers”, MJP Publishers, Chennai, 2011
2. Kothari C.R., “Research, Methodology - Method and Techniques”. New Age International (P) Ltd., New Delhi, Reprint 2003.
3. Doebelin, Ernest. O., “Engineering Experimentation: planning, execution, reporting”- Tata McGraw - Hill International edition, 1995.
4. Rao S.S. “Engineering Optimization:Theory and Practice”, John Wiley & Sons, 2009
5. Dan Jones, “Technical writing style”, Pearson Education Company, Massachusetts, 1998.
6. Abdul Rahim R., “Thesis writing: A Manual for Researchers”, New Age International (P) Ltd., 2005.

OUTCOMES :

- Plan, undertake, execute research projects and prepare relevant documents
- Take up doctoral research in their area of interest and submit the thesis and defend the same successfully

ECB6124	VLSI PHYSICAL DESIGN LAB	L	T	P	C
		0	0	3	1

OBJECTIVES:

- To gain hands-on experience on the VLSI physical design tools.
- To practice the VLSI Digital design flow using Cadence/Tanner/Mentor EDA tools.

FPGA based Experiments:

1. Design Entry Using Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.

ASIC based experiments:

1. ASIC RTL realization- Cadence/Tanner/Mentor Graphics.
2. Interpretation of standard cell library descriptions, Boolean optimization, optimization for area, power – Cadence/Tanner/Mentor Graphics.
3. Static Timing analyses procedures and constraints. Critical path considerations – Cadence/Tanner/Mentor Graphics.
4. Scan chain insertion, Floor Planning Routing and Placement procedures and alternatives. Back annotation, layout generation, LVS, Formal verification – Cadence/Tanner/Mentor Graphics.
5. LVS, Back annotation- Cadence/TANNER/ Mentor Graphics.

Total Hours : 45

OUTCOMES:

The students will have hands-on experience in

- development of digital integrated circuits design, implementation methodologies and testing.
- back-end design flow of Digital integrated circuits.

ECB6125	EMBEDDED SYSTEMS LAB	L	T	P	C
		0	0	3	1

OBJECTIVES:

- To gain the working knowledge of various embedded tools.
- To develop the various samples program for the Target processor like 8051 Microcontroller, PIC controller & ARM7 TDMI processor.
- To develop the simulation & debugging skills of various tools.

LIST OF EXPERIMENTS:

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers- Assembly and C Programming: I/O Programming, Timers.
2. Interrupts, Serial port programming with 8051/PIC Microcontrollers- Assembly and C programming.
3. PWM Generation, Motor Control, ADC/DAC with 8051/PIC Microcontrollers- Assembly and C programming.
4. LCD and RTC Interfacing, Sensor Interfacing with 8051/PIC Microcontrollers- Assembly and C programming
5. Design with 16 bit processors: I/O programming, Timers, Interrupts, Serial Communication
6. Design with ARM Processors: I/O programming, ADC/DAC, Timers, Interrupts
7. Study of one type of Real Time Operating Systems (RTOS)
8. Mini-project

OUTCOMES:

- The student will be able to program and test the working environment of Keil µvision, IAR embedded workbench and MPlab tools.

SEMESTER II

ECB6231	**ASIC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

OBJECTIVES:

To impart knowledge on

- the concept of structure and features Full custom and semicustom ASIC types.
- the fundamentals of digital logic design and the physical features of each ASIC.
- ASIC logic design, testing of physical design partitioning, floor planning, placement, and routing.

MODULE I INTRODUCTION TO ASICs, ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort – Library cell design.

MODULE II PROGRAMMABLE ASICs AND LOGIC CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III INTERCONNECTS AND LOW LEVEL DESIGN LANGUAGES 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language .

MODULE IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

MODULE V PARTITIONING, FLOOR PLANNING, PLACEMENT & ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

Total Hours : 45

REFERENCES :

1. H. Bhatnagar, “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime”, 2nd edition, 2001.
2. M.J.S .Smith, “Application Specific Integrated Circuits”, Addison -Wesley Longman Inc., 2003.
3. Keith Barr “ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits”, McGrawHill, 2006.
3. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
4. Steve Kilts, “Advanced FPGA Design”, Wiley Inter-Science, 2007.

OUTCOMES:

The students will be knowledgeable in

- the ASIC Design Flow and its Architecture.
- the Logic Synthesis and Testing methodologies.
- floor Planning and Physical Design Flows.

ECB6232 ANALOG INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

To make the student understand the design of

- different analog integrated circuits using CMOS.
- CMOS amplifiers, operational amplifier, PLL and switched capacitor circuits.

MODULE I INTRODUCTION **12**

Analog MOS transistor models Temperature effects and Noise in MOS transistor MOS resistors, characterization of resistive, capacitive elements and MOS devices. Passive and active CMOS current sink/ sources– basics of single stage CMOS amplifiers common Source, common gate and source follower stages frequency response.

MODULE II CMOS DIFFERENTIAL AMPLIFIERS **10**

CMOS Operational Amplifiers one stage and two stage gain boosting Common mode feedback (CMFB) Cascode and Folded cascade structures.

MODULE III HIGH PERFORMANCE OP-AMPS **12**

High speed/ high frequency op-amps, micro power op-amps, low noise op-amps and low voltage op-amps. Current mirrors, filter implementations. Supply independent and temperature independent references Band gap references PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits – effects due to nonlinearity and mismatch in MOS circuits.

MODULE IV SWITCHED CAPACITOR CIRCUITS **11**

First and Second Order Switched Capacitor Circuits, Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs non ideal effects in PLLs, Delay locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.

Total Hours : 45

REFERENCES:

1. David. A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2001.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuit”, Tata McGraw HILL, 2002.
3. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002.
4. Mohammed Ismail & Feiz, “Analog VLSI – Signal Information and Processing”, John Wiley and Sons.

OUTCOMES:

The students will be able to

- analyze the characteristics of different CMOS analog circuits.
- design of mixed signal circuits like ADC and DAC.

ECB6233 REAL TIME OPERATING SYSTEMS L T P C

3 0 0 3

OBJECTIVES:

- To provide the students with an understanding of the aspects of the Operating systems and Real-time Operating Systems
- Introduction to Resource management, time-constrained communication, scheduling and imprecise computations, real-time kernels and case studies.
- Comparison of various RTOS.

MODULE I REVIEW OF OPERATING SYSTEMS 9

Basic Principles - Operating System structures – System Calls – Files – Concurrent Execution & Interrupts- Processes – Design and Implementation of processes – Communication between processes-Process Scheduling.

MODULE II OVERVIEW OF RTOS 9

Real-time System: Hard versus Soft Real-time systems – examples-Difference between Traditional OS and RTOS. RTOS Kernel -RTOS Task and Task state Multitasking – Task Assignment, Task Priorities, Scheduling.

MODULE III IPC MECHANISMS 9

Intertask Communication & Synchronization – Definition of Context Switching, Critical Section – Re-entrant Functions, Deadlocks, Interprocess Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues.

MODULE IV REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Real Time Languages – RT scheduling -Interrupt processing -Control Blocks – Memory Requirements.

MODULE V REAL TIME KERNEL AND RTOS APPLICATION 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – µC/OS-II – RT Linux Case studies-RTOS for fault Tolerant Applications – RTOS for Control Systems.

Total Hours : 45

REFERENCES:

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
2. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
3. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
4. Charles Crowley, “Operating Systems-A Design Oriented approach” Tata McGraw Hill.

OUTCOMES:

After successful completion of the module, the students shall be able to

- understand the Embedded Real Time software that is needed to run embedded systems.
- illustrate the differences between various types of system software (real-time, information systems, fault tolerant).
- describe the common types of faults that occur in embedded systems.

ECB6234 ADVANCED EMBEDDED SYSTEMS L T P C

3 0 0 3

OBJECTIVES:

To impart knowledge on

- basics of Embedded hardware and software.
- power Optimization Techniques.
- various memory types and Interfacing Techniques.

MODULE I EMBEDDED HARDWARE AND SOFTWARE 9

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency – Interrupt routines in an RTOS environment –Hard Real-Time scheduling considerations - Embedded platform boot sequence.

MODULE II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9

Embedded systems, Hardware/Software Co-Design, Single-processor Architectures & Multi-Processor Architectures, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning, Hardware/Software Cost Estimation, Optimization.

MODULE III POWER OPTIMIZATION TECHNIQUES IN EMBEDDED SYSTEMS 9

The power profile of an Embedded Computing Systems – Constant versus Dynamic power – A simple model of power efficiency –Advanced Configuration and Power Interface –ACPI system states.

MODULE IV MEMORY AND INTERFACING 9

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing - communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration -Multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols

MODULE V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9

Modes of operation – Finite state machines – Models – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology – Automation synthesis – Hardware software co-simulation – IP cores .

Total Hours : 45

REFERENCES:

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.
2. Peter Barry, Patrick Crowley, “Modern Embedded Computing” Morgan Kaufmann Publishers, 2012.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
4. Frank Vahid and Tony Givargis ‘Embedded Systems Design: A Unified Hardware/Software Introduction’, John & Wiley Publications, 2002.
5. GiovanniDe Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann Publishers, 2001.

OUTCOMES:

Students will be knowledgeable in

- Hardware software co design and its issues.
- Hardware software partitioning and its concurrent design.

ECB6235	ANALOG IC DESIGN LAB	L	T	P	C
		0	0	3	1

OBJECTIVES :

Students will practice the

- Simulation of analog integrated circuits.
- Layouts design and compare with the schematic circuits.
- Parasitic extraction and simulation to verify the performance matches against specifications.

LIST OF EXPERIMENTS

1. Study of the Cadence design system tool.
2. Layout Design using LAY techniques.
3. MOS Device Characterization and parametric (PAR) analysis.
4. Current Mirrors: Simple, cascode, feedback and low-voltage.
5. Inverting Amplifiers: Current Mirror Load, Digital CMOS, PMOS with self biased load and self biased CMOS.
6. Differential Amplifiers: Simple and cascode current mirrors.
7. Operational Trans conductance Amplifiers (OTA): Symmetrical OTA.
8. Operational amplifiers (OP): Three stage OP-AMP.
9. The parametric (PAR) analysis Analog System: Continuous low pass filter.
10. Switched Capacitor Integrators: Use of transmission gates, capacitors and OP-AMP.

OUTCOMES:

On completion of the course, students will be able to use the following tools for designing analog integrated circuits.

- Composer (schematic capture).
- Virtuoso (layout generation).
- Analog Artist (simulation front-end).
- Spectre HDL (circuit simulation).
- Diva tools (DRC, LVS, ERC, extraction).
- Hierarchy Editor (parasitic simulation).
- Artist statistics (Monte Carlo Simulation and statistical analysis tools).

ECB6236	DESIGN / FABRICATION PROJECT	L	T	P	C
		0	0	3	1

OBJECTIVES :

To improve the professional competency and research aptitude by performing design and fabrication project. This design skill will help the students to develop the work practice to apply the design skills for real life problems.

The project can be a experimental project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project in the parent institute itself. Department will constitute an Evaluation Committee to review the project.

OUTCOMES:

At the end of the project the student will be able to design and fabricate the hardware.

SEMESTER III

ECB7102	PROJECT MANAGEMENT	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The objective of the course is to provide knowledge to students about the stages of a project and how each stage can be effectively managed and to impart design considerations of safety organization and control.

MODULE I **9**

Project definition, Project Profile and standards, Feed back information (MIS), Evaluation and Modification, Selection, Criteria.

MODULE II **9**

Planning the process, Strategic and Managerial Planning, Organising the process planning, cost and costing, Cost Control systems, Economic Balancing, Network Planning, Methods (PERT/CPM), Engineering Flow Diagrams, Cost requirements, Analysis and Estimation of Process Feasibilities (Technical/Economical) Analysis, Cost – Benefit Ratio Analysis, Project Budgeting, Capital Requirements, capital Market, Cash Flow Analysis, Break even strategies.

MODULE III **9**

Plant Engineering Management, Objectives, Programme, Control, Plant Location and Site Selection, Layout diagrams, Selection and procurement of equipment and machineries, Installation, Recommission, Commissioning and performance appraisal, Strategies choice and Influence, Product planning and development, Provision and maintenance of service facilities.

MODULE IV **9**

Process safety, Materials safety and Handling regulations, Safety in equipment and machinery operations, Design considerations of safety organization and control, Pollution, Pollution control and Abatement, Industrial Safety Standard Analysis.

MODULE V **9**

Government regulations on procurement of raw materials and its allocation. Export – Import regulations, Pricing policy, Industrial licensing procedure, Excise and other commercial taxes, Policies on depreciation and corporate tax, Labour laws, Social welfare legal measurements, Factory act, Regulations of Pollution Control Board.

Total Hours : 45

REFERENCES:

1. Cheremisinoff, N. P., Practical Guide to Industrial Safety: Methods for Process Safety Professionals, CRC Press, 2001
2. Couper, J. R., Process Engineering Economics, CRC Press, 2003.
3. Perry, J. H. “Chemical Engineer’s Hand Book”, 8th Ed., McGraw Hill, New York, 2007.
4. Peters, M. S., Timmerhaus, C. D. and West, R. E., “Plant Design and Economics for Chemical Engineers”, 5th Edn., McGraw Hill, 2003.
5. Silla, H., Chemical Process Engineering: Design and Economics, CRC Press, 2003.
6. Vinoski, W., Plant Management Handbook, Pearson Education, Limited, 1998.
7. Watermeyer, P., Handbook for Process Plant Project Engineers, John Wiley and Sons, 2002.

OUTCOMES:

At the end of the course the student will be able to

- to identify key components of a project
- describe the stages of a project and how each stage can be effectively managed.
- learn Design considerations of safety organization and control
- learn government regulations on procuring raw materials.

ELECTIVES

ECBY26 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- The Power analysis used in CMOS devices.
- Various techniques to reduce the power consumption in VLSI Circuits.
- Various Low power Architectures.

MODULE I DEVICE & TECHNOLOGY IMPACT ON LOW POWER 9

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

MODULE II SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS 9

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation -Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

MODULE III LOW POWER DESIGN 9

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre computation logic.

MODULE IV LOW POWER ARCHITECTURE &SYSTEMS 5

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

MODULE V LOW POWER CLOCK DISTRIBUTION 5

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co-design of clock network.

MODULE VI ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES 8

Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis

Total Hours : 45

REFERENCES:

1. Gary K. Yeap, Farid N. Najm, “Low power VLSI design and technology”, World Scientific Publishing Ltd., 1996.
2. Dimitrios Soudris, Christian Piguet, Costas Goutis, “Designing CMOS circuits for low power”, Kluwer Academic Publishers, 2002
3. Kaushik Roy and Sharat C. Prasad, “Low-Power CMOS VLSI Circuit Design”, Wiley-Interscience, 2000.
4. Chandrakasan, R. Brodersen, “CMOS Low Power Digital Design”, Kluwer Academic Publications, 1995.
5. Rabaey, M. Pedram, “Low Power Design Methodologies”, Kluwer Academic Publications, 1996.
6. Christian Piguet, “Low-power CMOS circuits: technology, logic design and CAD tools”, CRC Press, Taylor & Francis Group, 2006.

OUTCOMES:

The students will be knowledgeable in

- Static and dynamic power dissipation in integrated chips.
- Estimation of power for simple models.
- Low Power Dissipation Techniques in Clocking strategies and I/O circuits.

ECBY27 RF INTEGRATED CIRCUIT DESIGN L T P C

3 0 0 3

OBJECTIVES:

- The different RF transceiver architectures
- The methods of designing passive components in IC
- The design of LNA, Power amplifiers, PLL, Oscillators and frequency synthesizers.

MODULE I TRANSCEIVER ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures upconversion Transmitter.

MODULE II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

MODULE III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MODULE IV PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer- N frequency synthesizers, Direct Digital Frequency synthesizers.

MODULE V MIXERS AND OSCILLATORS **9**

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

Total Hours : 45

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

OUTCOMES:

Students will be knowledgeable in

- The design of different RF circuits used in the RF receivers
- The analysis of the different characteristics of RF circuits.

ECBY28 ADVANCED MICROPROCESSORS & MICRO CONTROLLERS **L T P C 3 0 0 3**

OBJECTIVES:

- To familiarize with advanced computer architecture concepts.
- To learn about Design and programming of high performance CISC and RISC Microprocessor Architectures.
- To learn about Design and programming of RISC type Micro controller Architectures.
- To learn about Design and programming of MSP 430 microcontroller.

MODULE I MICROPROCESSOR ARCHITECTURE 6

Instruction set - Data formats - Instruction formats - Addressing modes - Memory Hierarchy - register file - Cache - Virtual memory and paging – Segmentation.

MODULE II PIPELINING AND COMPUTER PRINCIPLES 6

Pipelining - The instruction pipeline - pipeline hazards - Instruction level parallelism - reduced instruction set - Computer principles - RISC versus CISC - RISC properties - RISC evaluation - On-chip register files versus cache evaluation.

MODULE III HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 6

The software model - functional description - CPU pin descriptions - RISC concepts - bus operations - Super scalar architecture - pipe lining - Branch prediction - The instruction and caches - Floating point unit.

MODULE IV OPERATING MODES OF PENTIUM AND PROGRAMMING 7

Protected mode operation - Segmentation - paging - Protection - multitasking - Exception and interrupts - Input/Output - Virtual 8086 model - Interrupt processing - Instruction types - Addressing modes - Processor flags - Instruction set - Basic programming the Pentium Processor.

MODULE V HIGH PERFORMANCE RISC ARCHITECTURE 10

ARM: The ARM architecture - ARM organization and implementation - The ARM instruction set - The thumb instruction set - Basic ARM Assembly language program - ARM CPU cores.

MODULE VI MICRO CONTROLLER 10

CPU Architecture - Instruction set - Interrupts - Timers - Memory - I/O port expansion - I2C bus for peripheral chip access - A/D converter – UART, MSP430 architecture, instruction set and programming.

Total Hours : 45

REFERENCES:

1. Daniel Tabak, “Advanced Microprocessors”, McGraw Hill. Inc., 1995.
2. James L. Antonakos, “The Pentium Microprocessor”, Pearson Education, 1997.
3. Steave Furber, “ARM system - on - chip architecture”, Addison Wesley, 2000.
4. John.B..Peatman, “Design with PIC Micro controller”, Pearson Education, 1988.
5. Gene. H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
6. James L Antonakos, “An Introduction to the Intel family of Microprocessors”, Pearson education, 1999.
7. Barry B. Brey, “The Intel Microprocessors Architecture, Programming and Interfacing”, PHI, 2002.

OUTCOMES:

Students will be able to

- Understand Advanced computer architecture concepts
- Know the functionality of advanced Microprocessors and Microcontrollers
- Write basic programs in PENTIUM, ARM, MSP 430.
- Design and develop microprocessor/microcontroller based system for various applications

ECBY29	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- VLSI layout design rules and translate circuit concepts onto silicon.
- Floor planning concepts in back end designs.

MODULE I VLSI DESIGN METHODOLOGIES **11**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Introduction to CAD tools - Evolution of Design Automation-Basic Transistor Fundamentals-CMOS realizations of basic gates - Modeling techniques, Types of CAD tools.

MODULE II DESIGN RULES **8**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.

MODULE III FLOOR PLANNING **8**

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

MODULE IV SIMULATION **9**

Introduction to logic simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

MODULE V MODELING AND SYNTHESIS **9**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations. Introduction to Reconfigurable computing, FPGAs, the Altra Quartus II flow.

Total Hours : 45

REFERENCES:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley & Sons, 2002.
2. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic Publishers, 2002.
3. Verilog HDL, Samir Palnitkar, Second Edition, Pearson Education, 2004.
4. Verilog HDL Synthesis, J.Bhaskar, BS publications, 2001.

OUTCOMES:

Students will be knowledgeable in

- Identifying the best approach algorithm to optimize circuits at different levels of design.
- Applying the algorithms in the back end flow to optimize the circuits for maximum speed and area.

ECBY30 RECONFIGURABLE COMPUTING L T P C

3 0 0 3

OBJECTIVES:

- Students will be able to investigate the state-of-the-art in reconfigurable computing both from a hardware and software perspective.
- Students will understand both how to architect reconfigurable systems and how to apply them to solving challenging computational problems.
- Specific contemporary reconfigurable computing systems are examined to identify existing system limitations and to highlight opportunities for research in dynamic and partial configuration areas.

MODULE I INTRODUCTION 9

Introduction, origin of reconfigurable computing, Reconfigurable computing architecture, Reconfigurable computing hardware, Logic—The Computational Fabric, The Array and Interconnect, Extending Logic, Configuration, Case Studies, Altera Stratix, Xilinx Virtex-II Pro.

MODULE II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable Processing Fabric Architectures, RPF Integration into Traditional Computing Systems, Reconfigurable computing systems, Early Systems, PAM, VCC, and Splash , Small-scale Reconfigurable Systems, Circuit Emulation, Accelerating Technology, Reconfigurable Supercomputing, Other System Issues, The Future of Reconfigurable Systems.

MODULE III PROGRAMMING RECONFIGURABLE SYSTEMS, COMPUTATION MODELS AND SYSTEM ARCHITECTURES 9

Computation Models -- Challenges, Common Primitives, Dataflow, Sequential Control, Data Parallel, Data-centric , Multi-threaded, Other Compute Models, System Architectures - Streaming Dataflow, Sequential Control, Bulk Synchronous Parallelism, Data Parallel, Cellular Automata, Multi-threaded, Hierarchical Composition.

MODULE IV FPGA DESIGN **9**

FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

MODULE V APPLICATION DEVELOPMENT **9**

Implementing Applications with FPGAs, Strengths and Weaknesses of FPGAs, Application Characteristics and Performance, General Implementation Strategies for FPGA-based Systems, Implementing Arithmetic in FPGAs, Hardware/Software Partitioning.

Total Hours : 45

REFERENCES:

1. Scott Hauck, André DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation” , Morgan Kauffman publishers, 2008.
2. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
3. C. Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2007.
4. P. Lysaght and W. Rosenstiel, “New Algorithms, Architectures and Applications for Reconfigurable Computing”, Springer, 2005.
5. W. Wolf, “FPGA Based System Design”, Prentice-Hall, 2004.

OUTCOMES:

The students will understand

- various Reconfigurable Computing architectures systems
- and will have an overview about the Programming model for Reconfigurable computing
- reconfigurable computing design on FPGA
- few applications of RC and study its impact on hardware and software partitioning.

ECBY31 TESTING OF VLSI CIRCUITS L T P C

3 0 0 3

OBJECTIVES:

- Automated and manual techniques for generating tests for faults in digital circuits and systems.
- Generation of test vectors for combinational and sequential circuits
- Fault diagnosis algorithms

MODULE I BASICS OF TESTING AND FAULT MODELING 9

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

MODULE II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

MODULE III DESIGN FOR TESTABILITY 9

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design – System level DFT approaches.

MODULE IV SELF TEST AND TEST ALGORITHMS 9

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design – Testing of Embedded RAMs.

MODULE V FAULT DIAGNOSIS 9

Logic Level Diagnosis - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

Total Hours : 45

REFERENCES:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems and Testable Design”, Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L. Crouch, “Design Test for Digital ICs and Embedded Core Systems”, Prentice Hall International, 2002.

OUTCOMES:

Students will be knowledgeable in

- principles of testing digital systems.
- design for testability in combinational and sequential circuits.
- basics of self test and fault diagnosis.

ECBY32 CMOS MIXED SIGNAL CIRCUIT DESIGN L T P C

3 0 0 3

OBJECTIVES:

- The different mixed-signal circuit design methodologies.
- The design of sampling circuits and integrator.

MODULE I PLL AND SWITCHED CAPACITOR CIRCUITS 9

Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL- Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

MODULE II SAMPLING CIRCUITS 9

Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

MODULE III DAC 9

Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

MODULE IV ADC 9

Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures, pipelined architectures, Successive approximation architectures, interleaved architectures.

MODULE V FILTERS **9**

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

Total Hours : 45

REFERENCES:

1. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, 2001.
2. Razavi, “Principles of data conversion system design”, S.Chand and company ltd, 2000.
3. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2002.
4. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 1987.
5. Baker, Li, Boyce, “CMOS : Circuit Design, layout and Simulation”, PHI, 2000.

OUTCOMES:

Students will be able to

- analyze the characteristics of different mixed-signal circuits.
- design of mixed signal circuits like ADC and DAC

ECBY33 EMBEDDED NETWORKING L T P C

3 0 0 3

OBJECTIVES:

- To study the concepts of embedded networking.
- To explore various bus architectures.
- To explore the fundamentals of embedded security.

MODULE I THE AUTOMOTIVE CAN BUS 9

Introduction-Concepts of Bus Access and arbitration –error processing and management –definition of the CAN protocol ISO 11898-1-error properties-detection and processing –framing, signal propagation-Bit synchronization-high speed CAN –low speed CAN-CAN components and development tools for CAN.

MODULE II USB 6

Introduction - types of USB transfers-bulk transfer –interrupt transfer-isochronous transfer-introduction to enumeration process –descriptors.

MODULE III INDUSTRIAL NETWORKING PROTOCOL 9

LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audio-video buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'-profi bus.

MODULE IV ETHERNET BASICS 6

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

MODULE V BLUETOOTH AND ZIGBEE 6

Bluetooth: Specifications- Bluetooth Radio- Type of Antenna, Antenna Parameters- Bluetooth Networking- Connection establishment procedure, Profile and usage model - Wireless networking, wireless network types, devices

roles and states – IEEE 802.15.4 –Zigbee specifications- Zigbee stack protocol stack-PAN formation.

MODULE VI RF COMMUNICATION 6

Adhoc network, scatter net- GSM- Overview of IrDA, HomeRF, Wireless LANs- IEEE 802.11x - NFC (near-field communication)- Wireless sensor networks – Introduction – Applications.

Total Hours : 45

REFERENCES:

1. Dominique Paret, “Multiplexed Networks for Embedded Systems”, Wiley 2007.
2. Jan Axelson, “USB Complete”, Lakeview Research, 2005.
3. Jan Axelson, “Embedded Ethernet Complete”, Lakeview Research, 2005.
4. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded networking with CAN and CAN open”. Embedded System Academy 2005.
5. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2005.
6. C.S.R. Prabhu and A.P. Reddi, “Bluetooth Technology and its Applications with JAVA and J2EE, PHI”, 2006.
7. Rappaport Theodore S, “Wireless Communications: Principles And Practice”, Pearson Education, 2010.
8. Shahin Farahani,”ZigBee Wireless Networks and Transceivers”, Newnes Publications, 2008.

OUTCOMES:

The student achieve knowledge and skills on the following

- proper understanding of what constitute networking and its significance in embedded systems
- able to create embedded Ethernet
- ability and skill to use appropriate interfaces, protocols and buses in embedded networking.

ECBY34	RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the differences between CISC and RISC Processor.
- To study the advanced processor family architectures like AVR, MSP430 and ARM.
- To gain knowledge of Assembly language programming in ARM Processor.
- To introduce ARM application development.

MODULE I AVR MICROCONTROLLER ARCHITECTURE 9

Architecture – memory organization – addressing modes – instruction set – programming techniques –Assembly language & C programming- Development Tools – Cross Compilers – Hardware Design Issues .

MODULE II MSP430 ARCHITECTURE 9

Architecture – CPU features – Memory structure - Interrupts – Input and Output – On-chip peripherals – Addressing modes – Instruction sets – Hardware considerations – Flash memory – Low power design.

MODULE III ARM ARCHITECTURE AND PROGRAMMING 9

ARM processor fundamentals – Registers – Pipeline – Exceptions - Interrupts –core extension- Instruction set – Thumb instruction set - 'C' programming – writing and optimising ARM assembly code – Instruction scheduling – Register allocation – conditional execution – Looping constraints.

MODULE IV ARM APPLICATION DEVELOPMENT 9

Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Example: Standalone - Embedded Operating Systems – Fundamental Components - Example Simple little Operating System.

MODULE V DESIGN WITH ARM MICROCONTROLLERS 9

Integrated development environment – Standard I/O Libraries - User Peripheral Devices – Application of ARM processor: Wireless Sensor Networks.

Total Hours : 45

REFERENCES:

1. Steve Furber, “ARM system on chip architecture”, Addison Wesley, 2000.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier 2007.
3. Trevor Martin, “The Insider's Guide To The Philips ARM7-Based Microcontrollers, An Engineer's Introduction To The LPC2100 Series”, Hitex (UK) Ltd.,
4. Dananjay V. Gadre “Programming and Customizing the AVR microcontroller”, McGrawHill 2001
5. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier 2003.
6. ARM Architecture Reference Manual
7. LPC213x User Manual

OUTCOMES:

The students will understand:

- AVR, MSP430 and ARM architectures and to program in both assembly and C language.
- various tools like WinAVR, IAR Embedded workbench and real-time application programming with it.

ECBY35 DISTRIBUTED EMBEDDED COMPUTING L T P C

3 0 0 3

OBJECTIVES:

- The various hardware and software architectures used for distributed embedded computing.
- Distributed computing system models and Distributed databases.
- The infrastructure required to support an Internet connection, uses of common Internet protocols, and basic principles of the DNS.
- The distributed computing technologies.

MODULE I THE HARDWARE INFRASTRUCTURE 9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – wide Area Networks – Network management – Network Security – Cluster computers.

MODULE II INTERNET CONCEPTS 9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

MODULE III DISTRIBUTED COMPUTING USING JAVA 9

I/O streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

MODULE IV EMBEDDED AGENT 9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

MODULE V EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

Total Hours : 45

REFERENCES:

1. Dietel & Dietel, “JAVA-How to program”, Prentice Hall 1999.
2. SapeMullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – Concepts and Design”, Addison Wesley 1988.
4. Bernd Kleinjohann “Architecture and Design of Distributed Embedded Systems”, C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

OUTCOMES:

The students will be knowledgeable in

- designing and analyzing high-performance computer system.
- selecting the suitable embedded architecture.

ECBY36 DESIGN OF SEMICONDUCTOR MEMORIES

L	T	P	C
3	0	0	3

OBJECTIVES:

- To study the concepts of random access memory and nonvolatile memories.
- To learn the implementation methods and problems in designing and making semiconductor memories.
- To understand different fault modeling and testing techniques.

MODULE I STATIC RANDOM ACCESS MEMORY TECHNOLOGY 4

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAM

MODULE II DYNAMIC RANDOM ACCESS MEMORY TECHNOLOGY 5

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures -BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

MODULE III NONVOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS, PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

MODULE IV MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

MODULE V RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

MODULE VI PACKAGING TECHNOLOGIES 9

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto-resistive. Random Access Memories (MRAMs) -Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Total Hours : 45

REFERENCES:

1. Ashok K.Sharma, “Semiconductor Memories Technology, Testing and Reliability”, Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3. Betty Prince, “Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

OUTCOMES:

The students will be able to

- design MOS memories.
- design memory fault modeling and memory design test-abilities.

ECBY37	CONTROL AREA NETWORK	L	T	P	C
		3	0	0	3

OBJECTIVES:

The student learn,

- the requirements of Embedded Networks
- CAN open configuration
- CAN controller overview and Implementation
- CAN Development Tools

MODULE I EMBEDDED NETWORK REQUIREMENTS **9**

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

MODULE II CAN OPEN **9**

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

MODULE III CAN **9**

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

MODULE IV IMPLEMENTATION OF CAN OPEN **9**

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.

MODULE V ISSUES **9**

Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

Total Hours : 45

REFERENCES:

1. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.
2. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2005.
3. Mohammed Farsi, Barbosa, “CANopen Implementation : Applications to Industrial Networks (Industrial Control, Computers, and Communications Series,18),Research Studies Press, 2000
4. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2007.

OUTCOMES:

The students will understand,

- the CAN message format.
- to select a CAN controller.
- CAN Implementation method and CAN Issues.
- the different types of noise commonly found in computer network.

ECBY38 INTRODUCTION TO MEMS SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

- This course is an introduction to MEMS, which also uses micro electronics. This course fulfils the need of electronic engineer who wants to create MEMS devices in the field of Mechanical, Electronic Sensors, Optical and RF system.

MODULE I INTRODUCTION TO MEMS **9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication.

MODULE II MECHANICS FOR MEMS DESIGN **9**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics - actuators, force and response time, Fracture and thin film mechanics.

MODULE III ELECTRO STATIC DESIGN **9**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

MODULE IV CIRCUIT AND SYSTEM ISSUES **9**

Electronic Interfaces, Feedback systems, Noise , Circuit and system issues, Case studies - Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

MODULE V INTRODUCTION TO OPTICAL AND RF MEMS **9**

Optical MEMS - System design basics - Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS - design basics, case study - Capacitive RF MEMS switch, performance issues.

Total Hours : 45

REFERENCES:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000.
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton, 2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

OUTCOME:

- At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

ECBY39 APPLICATIONS OF MEMS TECHNOLOGY L T P C

3 0 0 3

OBJECTIVES:

To Learn,

- the principles of micro-fabrication to the development of micromechanical devices and the design of Microsystems.
- the principles of energy transduction, sensing and actuation on a microscopic scale.
- modeling and Analysis of micro electromechanical devices and systems.

MODULE I MEMS: MICRO-FABRICATION, MATERIALS AND ELECTROMECHANICAL CONCEPTS 9

Overview of micro fabrication - Silicon and other material based fabrication processes - Concepts: Conductivity of semiconductors-Crystal planes and orientation-stress and strain-flexural beam bending analysis-torsional deflections-Intrinsic stress- resonant frequency and quality factor.

MODULE II ELECTROSTATIC SENSORS AND ACTUATION 9

Principle, material, design and fabrication of parallel plate capacitors as electrostatic sensors and actuators-Applications.

MODULE III THERMAL SENSING AND ACTUATION 9

Principle, material, design and fabrication of thermal couples, thermal bimorph sensors, thermal resistor sensors-Applications.

MODULE IV PIEZOELECTRIC SENSING AND ACTUATION 9

Piezoelectric effect-cantilever piezo electric actuator model-properties of piezoelectric materials- Applications.

MODULE V CASE STUDIES 9

Piezo resistive sensors, Magnetic actuation, Micro fluids applications, Medical applications, Optical MEMS.

Total Hours : 45

REFERENCES:

1. Chang Liu, "Foundations of MEMS", Pearson International Edition, 2006.
2. Marc Madou , "Fundamentals of microfabrication",CRC Press, 1997.
3. Boston , "Micromachined Transducers Source book",WCB McGraw Hill, 1998.
4. M.H.Bao "Micromechanical Transducers :Pressure sensors, accelerometers and gyroscopes", Elsevier, Newyork, 2000.

OUTCOME:

- At the end of this course, the student will have knowledge on MEMS materials, fabrication and their applications.

ECBY40 HARDWARE-SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

To Learn

- the basics of hardware software Co-design concepts.
- the use of OOP in the Co-Design process.

MODULE I INTRODUCTION **12**

Motivation hardware & software co-design, system design consideration, research scope & overviews Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development

MODULE II CO-DESIGN CONCEPTS **11**

Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software tradeoffs, co-design.

MODULE III METHODOLOGY FOR CO-DESIGN **12**

Amount of unification, general consideration & basic philosophies, a framework for co-design Unified Representation for Hardware & Software: Benefits of unified representation, modeling concepts. An Abstract Hardware & Software Model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model Performance Evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation.

MODULE IV OBJECT ORIENTED TECHNIQUES IN HARDWARE DESIGN 10

Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Total Hours : 45

REFERENCES:

1. Sanjaya Kumar, James H. Ayler “The Co-design of Embedded Systems: A Unified Hardware Software Representation”, Kluwer Academic Publisher, 2002.
2. H. Kopetz, “Real-Time Systems”, Kluwer, 1997.
3. R. Gupta, “Co-synthesis of Hardware and Software for Embedded Systems”, Kluwer 1995.
4. S. Allworth, “Introduction to Real-time Software Design”, Springer-Verlag, 1984.
5. C. M. Krishna, K. Shin, “Real-time Systems”, Mc-Graw Hill, 1997
6. Peter Marwedel, G. Goosens, “Code Generation for Embedded Processors”, Kluwer Academic Publishers, 1995.

OUTCOMES:

The student will be knowledgeable in

- the basic design methodologies used in the hardware software co-design
- the object oriented techniques in Hardware Design

ECBY41	SYSTEM VERILOG	L	T	P	C
		3	0	0	3

OBJECTIVES:

To Learn

- the basics of functional verification languages.
- the system verilog language constructs and the functional verification procedures.

MODULE I INTRODUCTION TO FUNCTIONAL VERIFICATION LANGUAGES 10

Introduction to System Verilog, System Verilog data types. System Verilog procedures, Interfaces and modports, System Verilog routines.

MODULE II INTRODUCTION TO OBJECT ORIENTED PROGRAMMING 11

Classes and Objects, Inheritance, Composition, Inheritance v/s composition, Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs.

MODULE III SYSTEM VERILOG ASSERTIONS 12

Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing.

MODULE IV COVERAGE DRIVEN VERIFICATION AND FUNCTIONAL COVERAGE IN SV 12

Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis SV and C interfacing: Direct Programming Interface (DPI)

Total Hours : 45

REFERENCES:

1. Sutherland, Stuart, Davidmann, Simon, Flake “SystemVerilog for Design” : A Guide to Using SystemVerilog for Hardware Design and Modeling, Peter 2nd ed., 2006

2. Chris Spear "SystemVerilog for Verification": A Guide to Learning the Testbench Language Features, 2006

3. Mintz, Mike, Ekendahl, Robert "Hardware Verification with System Verilog": An Object-Oriented Framework 2007

4. Bergeron, Janick "Writing Testbenches using SystemVerilog" 2006.

5. Meyyappan Ramanathan "A Practical Guide for SystemVerilog Assertions".

OUTCOMES:

The student will be knowledgeable in

- the verification of digital systems using system verilog.
- the convergence driven verification procedures.

ECBY42 SOC DESIGN AND VERIFICATION

L	T	P	C
3	0	0	3

OBJECTIVES:

To Learn

- the process of designing SOC and verification.
- basic SOC communication architectures.

MODULE I SYSTEM ON CHIP DESIGN PROCESS **12**

A canonical SoC Design, SoC Design flow waterfall vs spiral, topdown vs Bottom up. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure,Logic design issues Verification strategy, Onchip buses and interfaces, Low Power, Manufacturing test strategies.

MODULE II MACRO DESIGN PROCESS **11**

Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design,System Integration with reusable macros.

MODULE III SOC VERIFICATION **12**

Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM.

MODULE IV DESIGN OF COMMUNICATION ARCHITECTURES FOR SOCS **10**

On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

Total Hours : 45

REFERENCES:

1. Prakash Rashinkar Peter Paterson and Leena Singh “SoC Verification Methodology and Techniques”, Kluwer Academic Publishers, 2001.
2. Michael Keating, Pierre Bricaud, “Reuse Methodology manual for System on AChip Designs”, Kluwer Academic Publishers, second edition, 2001.
3. William K. Lam, “Design Verification: Simulation and Formal Method based Approaches”, Prentice Hall.
4. Rochit Rajsuman, “System- on -a- Chip Design and Test”, ISBN.
5. A.A. Jerraya, W.Wolf “Multiprocessor Systemsonchips”, M K Publishers.
6. Dirk Jansen “The EDA HandBook”, , Kluwer Academic Publishers.

OUTCOMES:

The student will be knowledgeable in

- The design of SOC and verification of SOC cores.
- The standard SOC communication architectures.

ECBY43 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN **L T P C**

3 0 0 3

OBJECTIVES:

To learn

- analyzing high speed circuits with signal behavior modeling
- signal integrity concepts
- analyze signal measurements
- clock distributions and clock oscillators

MODULE I SIGNAL PROPAGATION ON TRANSMISSION LINES **7**

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters.

MODULE II PRINTED CIRCUIT BOARDS **7**

PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

MODULE III MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS TALK **9**

Multi-conductor transmission-lines, coupling physics, per MODULE length parameters, Near and far-end cross-talk, minimizing cross-talk (stipline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

MODULE IV NON-IDEAL EFFECTS **7**

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tan d, routing parasitic,Common-mode current, differential-mode current, Connectors.

MODULE V POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

MODULE VI CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 6

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

Total Hours : 45

REFERENCES:

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified, Prentice Hall PTR, 2003.

OUTCOMES:

The students will be knowledgeable in

- signal behavior on high speed circuits such as cross talk in transmission lines
- power consideration and timing analysis and other losses in system design
- measurements in clock oscillators

ECBY44	OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

To learn

- the statistical modeling and test generation patterns
- placement and power estimation
- convex optimization techniques
- fundamentals of generic algorithms

MODULE I STATISTICAL MODELING **7**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

MODULE II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS **7**

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

MODULE III CONVEX OPTIMIZATION **8**

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max- monomial fitting, Posynomial fitting.

MODULE IV GENETIC ALGORITHM **8**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation-Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-

local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

MODULE V GENETIC ENCODING 7

Hybrid genetic-genetic encoding- Local Improvement - WDFR- Comparison of Gas- Standard cell Placement- GASP Algorithm- Unified Algorithm.

MODULE VI GA ROUTING PROCEDURES AND POWER ESTIMATION 8

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

Total Hours : 45

REFERENCES:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI:Timing and Power”, Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design, Layout and test Automation”, Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University Press, 2004.

OUTCOMES:

The students will be knowledgeable in

- Optimization techniques to improve the implementation of VLSI designs
- Genetic algorithms to solve the problems
- Statistical modeling in one or more disciplines.

ECBY45 VLSI SIGNAL PROCESSING L T P C

3 0 0 3

OBJECTIVES:

- To learn a complete DSP system and fundamentals of pipelining and parallel processing on FIR filters
- To study the concepts of retiming, unfolding, transforms and rank order filters.
- To understand different fast convolution algorithms and pipelining/parallel processing techniques for IIR filters
- To study different bit level architectures and their complexities
- To study the need for low power VLSI design principles applicable to VLSI signal processing

MODULE I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems , Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

MODULE II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture

MODULE III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

MODULE IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

MODULE V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

Total Hours : 45

REFERENCES:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

OUTCOMES:

The students will

- understand various algorithms that can be designed and applied on application specific VLSI architecture
- have the knowledge on fast convolution algorithms and high speed multipliers, used to improve the efficiency of DSP processors
- analyze different number representations, arithmetic based binary representations and complexities involved in it for easier numerical computations on processors.
- gain minimum knowledge to find solution for any research queries on DSP processors.

ECBY46	EVOLUTIONARY COMPUTATION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- This course will cover advanced topics in evolutionary algorithms and their application to open-ended computational design.
- Explore a variety of evolutionary approaches for problem
- Explore solution approaches and algorithms for determining feasible and optimal solutions.

MODULE I EVOLUTIONARY COMPUTING **9**

Introduction to Evolutionary Computation- Generic Evolutionary Algorithm-Representation-Initial Population-Fitness Function-Selection-Reproduction Operators-Stopping Conditions-Canonical Genetic Algorithm-crossover-Mutation-Control Parameters-Genetic Algorithm Variants.

MODULE II EVOLUTIONARY STRATEGIES AND EVOLUTIONARY PROGRAMMING **9**

Generic Evolution Strategy-Evolution Strategy Parameters-Strategy Operators-Strategy Variants-Basic Evolutionary Programming-Evolutionary Programming Operators-Strategy Parameters-Strategy Programming Implementations.

MODULE III GENETIC PROGRAMMING **9**

Tree Based Representation-Initial Population-Fitness Function-Crossover Operators-Mutation Operators –Constraint Handling-Multi Objective Optimization-Coevolution-Coevolution Types-Competitive Coevolution-Cooperative Coevolution.

MODULE IV SWARM INTELLIGENCE **9**

Social Behaviour as Optimization-Culture in Theory and Practice-Adaptive Cultural Model-The Particle Swarm-SocioCognitive UnderPinnings-A model of Binary Decisions-Particle Swarm in continuous numbers-Hybrid Evolution particle swarm.

MODULE V PARTICLE SWARM OPTIMIZATION AND ANT COLONY OPTIMIZATION 9

Particle Swarm Optimization-Basic Particle Swarm Optimization-Social Network Structure-Basic PSO Variants-Basic PSO Parameters-Single Solution Particle Swarm Optimization-Constraint Handling-Multi Objective Optimization-Ant Algorithms-Ant Colony Optimization Metaheuristics-Cemetry Organization and Brood Care-Division and Labor- Multi Objective Optimization-Evolving Neural Networks with Particle Swarm.

Total Hours: 45

TEXTBOOKS

1. David E. Goldberg, Addison, Genetic Algorithms in Search, Optimization and Machine Learning, Wesley, 1989.
2. A.E. Eiben and J. E. Smith, Introduction to Evolutionary Computing, Springer, 2003.
3. Riccardo Poli, William Langdon, and Nicholas McPhee,A Field Guide to Genetic Programming, Springer, 2008.
4. Andries P.Engelbrecht, Computational Intelligence an Introduction. John Wiley and Sons, 2007.

REFERNECES:

1. M. Dorigo and T. Stützle, Ant Colony Optimization, MIT Press, 2004.
2. M. Dorigo, G. Di Caro, M. Sampels (Eds.), Ant Algorithms, Springer, 2002.
3. R. Eberhart, Y. Shi, and J. Kennedy, Swarm intelligence, Morgan Kaufmann, 2001.
4. M. Resnick, Turtles, termites, and traffic jams, MIT Press, 1997.
5. S. Luke, Essentials of Metaheuristics, 2010.
6. Z. Michalewicz. Genetic Algorithms + Data Structures = Evolution Programs. Springer-Verlag, Berlin, 3rd edition, 1996.

OUTCOMES:

On completion of this course, the students will be able to

- Formulate and assess problems in evolutionary computation.
- Assess the strengths and weaknesses of several approaches to evolutionary computation.
- Apply techniques in evolutionary computation to problems such as optimization, automatic programming, control, and biological modeling.
- Understand solution approaches and algorithms for determining feasible and optimal solutions.

ECBY01	DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

To study and to understand

- the concepts of image processing and related transforms.
- the image processing techniques for enhancement, restoration and compression.

MODULE I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Basics of visual perception, Psycho, visual model, Color image fundamentals, Brightness, contrast, hue, saturation, GB, HSI models, Image sampling & quantization.

MODULE II IMAGE TRANSFORMS 9

2D discrete transforms, DFT, DCT, WHT, KLT, DWT, Simulation of 2D transform by 1D transform.

MODULE III IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification and specification techniques, Noise distributions, Spatial averaging , Directional Smoothing , Median, Geometric mean, Harmonic Mean, Homomorphic filtering, Color image enhancement, Image degradation model – Unconstrained and constrained restoration, Inverse filtering, Removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations, Spatial transformations, Gray level interpolation.

MODULE IV IMAGE SEGMENTATION AND RECOGNITION 9

Edge detection, Image segmentation by region growing, region splitting& merging and edge linking, Image Recognition, Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Neural Network applications in image processing.

MODULE V IMAGE COMPRESSION 9

Need for image compression, Vector Quantization, Run Length Encoding, Shift codes Block Truncation Coding. DCT and Wavelet Transform coding, JPEG, MPEG Standards

Total Hours : 45

REFERENCES:

1. Rafael C. Gonzalez, Richard E.Woods, Digital Image Processing, Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, Fundamentals of Digital Image Processing, Prentice Hall of India, 2002.
3. David Salomon : Data Compression The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
4. Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, Digital Image Processing using MATLAB, Pearson Education, Inc., 2004.
5. William K.Pratt, Digital Image Processing, John Wiley, NewYork, 2002

OUTCOME:

- On completion, the students will be knowledgeable in the mathematical representation of images and digital image image processing methods.

SSBY01 SOCIETY, TECHNOLOGY AND SUSTAINABILITY

L	T	P	C
3	0	0	3

OBJECTIVES:

- Aware of new technologies through advances in Science and Engineering.
- To make them realise the profound impact on society.
- Understand the ethical issues raised by technological changes and its effect on society.
- To introduce students a broad range of perspectives on the adoption and use of technologies.
- To make them realize the need of sustainability in the context of emerging technologies.

MODULE I TECHNOLOGY AND ITS IMPACTS **9**

Origin and evolution of technologies – Nature of technology- Innovation – Historical Perspective of technology – Sources of technological change - Co-evolution of technology and economy – Scientific knowledge and technological advance – Science and Engineering aspects of Technology – Impact on the Society – Social and Ethical Issues associated with technological change – Social and environmental consequences - Impact of technological change on human life –Technology and responsibility – Technology and social justice.

MODULE II TECHNOLOGY AND ITS ADVANCEMENT **9**

Sociological aspects of technology – Ethics and technology – Technology and responsibility – International Economics, Globalisation and Human Rights – Sustainability and Technology – Population and environment - Technology, Energy and Environment – Organisations and technological change

MODULE III SOCIETY AND TECHNOLOGY **9**

Impact of technologies on contemporary society – Role of society in fostering the development of technology – Response to the adaption and use of technology – Impact of technology on developer and consumers – Technological change and globalisation.

MODULE IV IMPACT OF A SPECIFIC TECHNOLOGY ON HUMAN WELFARE **9**

Impact of the following technologies on Human life – Medical and Biomedical – Genetics Technology – Electronics and Communications – Electronic media Technology – Information Systems Technology – Nanotechnology – Space Technology and Energy Technology.

MODULE V THE IMPORTANCE OF SUSTAINABILITY **9**

Sustainability – A brief history – Concepts and contexts for sustainability – Ecological imbalance and biodiversity loss – Climate change – Population explosion. Industrial ecology – systems approach to sustainability – Green engineering and technology- sustainable design- sustainable manufacturing- Green consumer movements – Environmental ethics – Sustainability of the planet Earth – Future planning for sustainability.

Total Hours : 45

REFERENCES:

1. Volti Rudi, “Society and Technology Change”, 6th Edition, Worth publishers Inc, USA, 2009.
2. Arthur W.A, “The nature of Technology: What it is and how it evolves”, Free Press, NY, USA, 2009.
3. Winston M and Edelbach R, “Society, Ethics and Technology”, 3rd Edition, San Francisco, USA, 2005.
4. Martin A.A Abraham, ‘Sustainability Science and Engineering: Defining Principles’, Elsevier Inc, USA, 2006.
5. R.V.G.Menon, “Technology and Society”, Pearson Education, India, 2011.

OUTCOMES:

At the end of this course, the students will be able to

- understand the benefits of modern technology for the well-being of human life.
- connect sustainability concepts and technology to the real world challenges.
- find pathway for sustainable society.